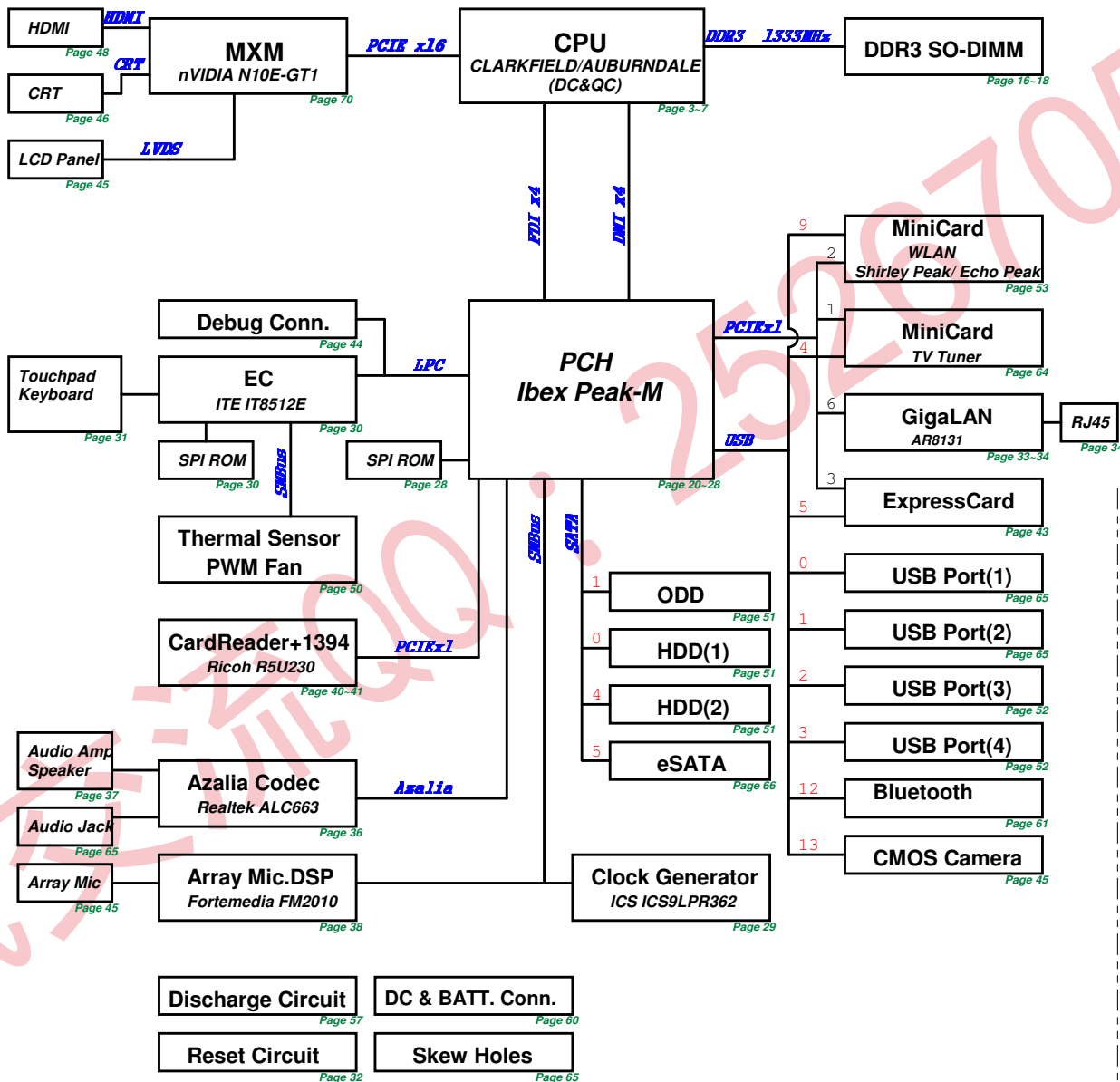


01. Block Diagram  
02. System Setting  
03. CPU(1)\_DMI, PEG, FDI, CLK, MISC  
04. CPU(2)\_DDR3  
05. CPU(3)\_CFG, RSVD, GND  
06. CPU(4)\_PWR  
07. CPU(5)\_XDP  
16. DDR3(1)\_SO-DIMM0  
17. DDR3(2)\_SO-DIMM1  
18. DDR3(3)\_CA/DQ Voltage  
19. VID Controller  
20. PCH(1)\_SATA, IHDA, RTC, LPC  
21. PCH(2)\_PCIE, CLK, SMB, PEG  
22. PCH(3)\_FDI, DMI, SYS\_PWR  
23. PCH(4)\_DP, LVDS, CRT  
24. PCH(5)\_PCI, NVRAM, USB  
25. PCH(6)\_CPU, GPIO, MISC  
26. PCH(7)\_POWER, GND  
27. PCH(8)\_POWER, GND  
28. PCH(9)\_SPI, SMB  
29. CLK\_IC93LPR362  
30. EC\_IT8512(1)  
31. EC\_IT8512(2)KB, TP, FP  
32. RST\_Reset Circuit  
33. LAN\_AR8131  
34. LAN\_RJ45  
36. AUD(1)\_ALC663VD  
37. AUD(2)\_AMP, JACK  
38. AUD(3)\_FM2010  
40. CB(1)\_R5U230  
43. CB(4)\_NewCard  
44. BUG\_Debug  
45. CRT(1)\_LVDS  
46. CRT(2)\_D-Sub  
47. CRT(3)\_Display Port  
48. TV(1)\_HDMI  
50. FAN\_Fan, Sensor  
51. XDD\_HDD, ODD  
52. USB\_USB Port  
53. MINICARD\_WLAN  
56. LED\_Indicator  
57. DSG\_Discharge  
60. DC\_DC/BAT CONN  
61. BT\_Bluetooth  
64. TUN\_TV Tuner  
65. ME\_CONN, Skew Hole  
66. ESA\_ESATA  
69. OTH\_GAME-LED  
70. VGA(1)\_MXM Slot  
71. VGA(2)\_LVDS Switch  
80. PWR(1)\_VCORE  
81. PWR(2)\_SYSTEM\_+12VSUS  
82. PWR(3)\_VTT\_CPUS & 1.05VS  
83. PWR(4)\_I/O\_DDR & VTT  
84. PWR(5)\_\*\*\*\*  
85. PWR(6)\_+1.8VS  
86. PWR(7)\_\*\*\*\*  
88. PWR(9)\_CHARGER  
90. PWR(11)\_DETECT  
91. PWR(12)\_LOAD SWITCH  
92. PWR(13)\_PROTECT  
93. PWR(14)\_SIGNAL  
94. PWR(15)\_FLOWCHART  
95. System History  
98. Power On Sequence  
99. Power On Timing

# G60J Schematics for Calpella Platform Rev. 1.5

## BLOCK DIAGRAM



PCH_IBEX GPIO					EC IT8512		EC IT8301	
PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power	EC GPIO	Use As	Signal Name	
GPIO 00	GPO	PCH_GPIO0_R	-	+3VS	GPIO0	O	PWR_LED#	
GPIO 01	-	-	INT TBD	+3VS	GPIO1	O	CHG_LED#	
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+5VS	GPIO2	-	-	
GPIO 06	GPI	DGPU_PWR_EN	INT TBD	+3VS	GPIO3	O	GAME_LED_EC#	
GPIO 07	-	-	INT TBD	+3VS	GPIO4	O	LCD_BL_PWM	
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS	GPIO5	O	FAN_PWM	
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS	GPIO6	-	-	
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS	GPIO7	O	SUSC_EC#	
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS	GPIO8	O	SUSB_EC#	
GPIO 12	Native	PM_LANPHY_EN	EXT PU	+3VSUS	GPIO9	-	-	
GPIO 13	-	-	-	+3VSUS	GPIO10	IO	SMB0_CLK	
GPIO 14	GPO	CB_SD#	EXT PU(DIODE DNI)	+3VSUS	GPIO11	IO	SMB0_DAT	
GPIO 15	GPO	WLAN_ON	INT PD	+3VSUS	GPIO12	O	A20GATE	
GPIO 16	GPO	DGPU_HOLD_RST#	-	+3VS	GPIO13	O	RCIN#	
GPIO 17	GPO	DGPU_PWROK	EXT PD & INT TBD	+3VS	GPIO14	O	PM_RSMRST#	
GPIO 18	Native	CLKREQ1_TV#	EXT PU(DNI)/PD	+3VS	GPIO15	-	-	
GPIO 19	GPI	SATA_DET#1_R	-	+3VS	GPIO16	IO	SMB1_CLK	
GPIO 20	Native	CLKREQ2_WLAN#	EXT PU(DNI)/PD	+3VS	GPIO17	IO	SMB1_DAT	
GPIO 21	GPI	SATA_DET#0_R	-	+3VS	GPIO18	O	PM_PWRBTN#	
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS	GPIO19	I	AC_IN_OC#	
GPIO 23	-	-	-	+3VS	GPIO20	O	OP_SD#	
GPIO 24	GPO	OC_LAN_RST#	EXT PU	+3VSUS	GPIO21	I	BAT1_IN_OC#	
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU(DNI)/PD	+3VSUS	GPIO22	I	RFOF_SW#	
GPIO 26	Native	CLKREQ4_ESATA#	EXT PU(Not used)	+3VSUS	GPIO23	I	PWRLIMIT#	
GPIO 27	-	-	INT WEAK PU	+3VSUS	GPIO24	I	PM_SUSC#	
GPIO 28	GPO	BT_LED/SPI_CS#2	EXT PD	+3VSUS	GPIO25	I	BUF_PLT_RST#	
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS	GPIO26	O	EXT_SCI#	
GPIO 30	Native	ME_SUSPWRDNACK / RTLAN_DSM#	EXT PU	+3VSUS	GPIO27	O	EXT_SMI#	
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS	GPIO28	O	LCD_BACKOFF#	
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS	GPIO29	I	FAN0_TACH	
GPIO 33	-	-	-	+3VS	GPIO30	-	-	
GPIO 34	Native	STP_PCI#	EXT PU	+3VS	GPIO31	O	VSUS_ON	
GPIO 35	Native	SATA_CLK_REQ#	EXT PU/PD(DNI)	+3VS	GPIO32	O	EGAD (IT8301 Address/Data connect)	
GPIO 36	GPO	DGPU_PWR_EN#	EXT PU	+3VS	GPIO33	O	EGCS# (IT8301 Cycle Start connect)	
GPIO 37	GPI	DGPU_PRSTN#	EXT PU	+3VS	GPIO34	O	EGCLK (IT8301 Clock connect)	
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS	GPIO35	I	PWR_SW#	
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS	GPIO36	I	LID_SW#	
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS	GPIO37	I	CAP_ACK#	
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS	GPIO38	-	-	
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS	GPIO39	I	EXP_GATE#	
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS	GPIO40	-	-	
GPIO 44	-	-	EXT PU (Not used)	+3VSUS	GPIO41	I	TP_CLK	
GPIO 45	-	-	EXT PU (Not used)	+3VSUS	GPIO42	IO	TP_DAT	
GPIO 46	-	-	EXT PU (Not used)	+3VSUS	GPIO43	O	THRO_CPU	
GPIO 47	Native	CLKREQ_PEG#	EXT PD	+3VSUS	GPIO44	IO	H_PECI	
GPIO 48	-	-	-	+3VS	GPIO45	-	-	
GPIO 49	GPO	GPU_RST# / CRIT_TEMP_REP#_R	-	+3VS	GPIO46	I	PM_SUSB#	
GPIO 50	-	-	EXT PU (Not used)	+5VS	GPIO47	-	-	
GPIO 51	Native	PCI_GNT1#	INT PU	+3VS	GPIO48	-	-	
GPIO 52	GPO	DGPU_SELECT#	EXT PU	+5VS	GPIO49	IO	PM_CLKRUN#	
GPIO 53	-	-	INT PU	+3VS	GPIO50	-	-	
GPIO 54	-	-	-	+5VS	GPIO51	O	GF_X_VR_ON	
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS	GPIO52	O	BAT_LEARN	
GPIO 56	Native	CLKREQ_GLAN#	EXT PU(DNI)/PD	+3VSUS	GPIO53	O	HSCK	
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS	GPIO54	O	NUM_LED#	
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS	GPIO55	O	CAP_LED#	
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS	GPIO56	-	-	
GPIO 60	GPO	RTLAN_DSM_EN	EXT PU	+3VSUS	GPIO57	I	SUS_PWRGD	
GPIO 61	-	-	-	+3VSUS	GPIO58	I	ALL_SYSTEM_PWRGD	
GPIO 62	-	-	-	+3VSUS	GPIO59	I	VRM_PWRGD	
GPIO 63	-	-	-	+3VSUS	GPIO60	I	GF_X_VR	
GPIO 64	Native	CLK_OUT0	INT TBD	+3VS	GPIO61	I	ALS_AD	
GPIO 65	Native	CLK_OUT1	INT TBD	+3VS	GPIO62	-	-	
GPIO 66	-	-	INT TBD	+3VS	GPIO63	O	CPU_VRON	
GPIO 67	-	-	INT TBD	+3VS	GPIO64	O	PM_PWROK	
GPIO 72	-	-	-	+3VSUS	GPIO65	O	VSET_EC	
GPIO 73	-	-	EXT PU (Not used)	+3VSUS	GPIO66	O	ISET_EC	
GPIO 74	-	-	EXT PU (Not used)	+3VSUS	GPIO67	O	TP_LED	
GPIO 75	Native	SML1_DAT	EXT PU	+3VSUS	GPIO68	-	-	

EC GPIO	Use As	Signal Name
GPIO0	I	ME_PM_SLP_M#
GPIO1	I	ME_SUSPWRDNACK
GPIO2	-	-
GPIO3	-	-
GPIO4	I	ME_+VM_PWRGD
GPIO5	I	ME_PM_SLP_LAN#
GPIO6	O	ME_AC_PRESENT
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	O	ME_PWROK
GPIO13	-	-
GPIO14	O	ME_SLP_M_EC#
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

SM\_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2h )
SO-DIMM 0	1010000x ( A0h )
SO-DIMM 1	1010001x ( A4h )
CPU Thermal IC(G780)	1001100x ( 98h )
VGA Thermal IC(G781-1)	1001101x ( 9Ah )
VGA Thermal Sensor(NB9E-GE1)	1001111x ( 9Eh )
VID Controller ASM8272	0011011x ( 36h )
DSP FM2010	

PCIE 1	Minicard TV Tuner	USB 0	USB Port (1)
PCIE 2	Minicard WLAN	USB 1	USB Port (2)
PCIE 3	Newcard	USB 2	USB Port (3)
PCIE 4	N/A	USB 3	USB Port (4)
PCIE 5	PCIE to SATA (SR)	USB 4	CMOS Camera
PCIE 6	GLAN	USB 5	Newcard
PCIE 7	N/A	USB 6	Minicard TV Tuner
PCIE 8	N/A	USB 7	N/A
		USB 8	OLED
		USB 9	WLAN
		USB 10	N/A
		USB 11	USB Port (5)
		USB 12	Bluetooth
		USB 13	Finger Print

SATA0	SATA HDD(1)
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	SATA HDD(2)
SATA5	eSATA

PEGATRON Title : System Setting

Engineer: Kenny Wu

BU2PDI

Size C

Project Name G60J

Date: Friday, July 31, 2009

Sheet 2 of 99

Rev 1.4

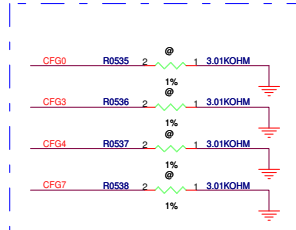
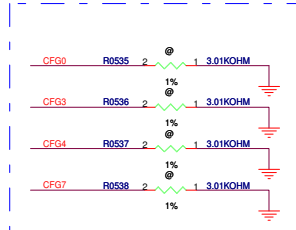
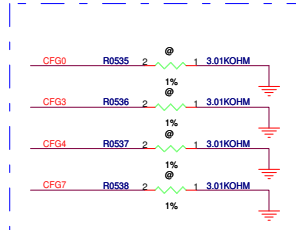
SM\_BUS ADDRESS :

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DSP FM2010	

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PCIE 2	Minicard WLAN	USB 1	USB Port (2)
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PCIE 4	N/A	USB 3	USB Port (4)
PCIE 5	PCIE to SATA (SR)	USB 4	CMOS Camera
PCIE 6	GLAN	USB 5	Newcard
PCIE 7	N/A	USB 6	Minicard TV Tuner
PCIE 8	N/A	USB 7	N/A
		USB 8	OLED
		USB 9	WLAN
		USB 10	N/A
		USB 11	USB Port (5)
		USB 12	Bluetooth
		USB 13	Finger Print



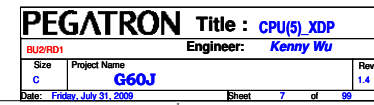




BU2/RD1		Engineer: <i>Kenny Wu</i>	
Size C	Project Name <b>G60J</b>	Rev 1.4	
Date: <u>Friday, July 31, 2009</u>		Sheet <u>5</u> of <u>99</u>	







图纸交流QQ : 252670528

PEGATRON		Title : NB(1) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009		Sheet	8 of 99



图纸交流QQ : 252670528

PEGATRON		Title : NB(2) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet	9	of 99

图纸交流QQ : 252670528

PEGATRON			Title :	NB(3) ****
BU2/RD1			Engineer:	Kenny Wu
Size	Project Name		Rev	
Custom	G60J		1.4	
Date:	Friday, July 31, 2009	Sheet	10	of 99

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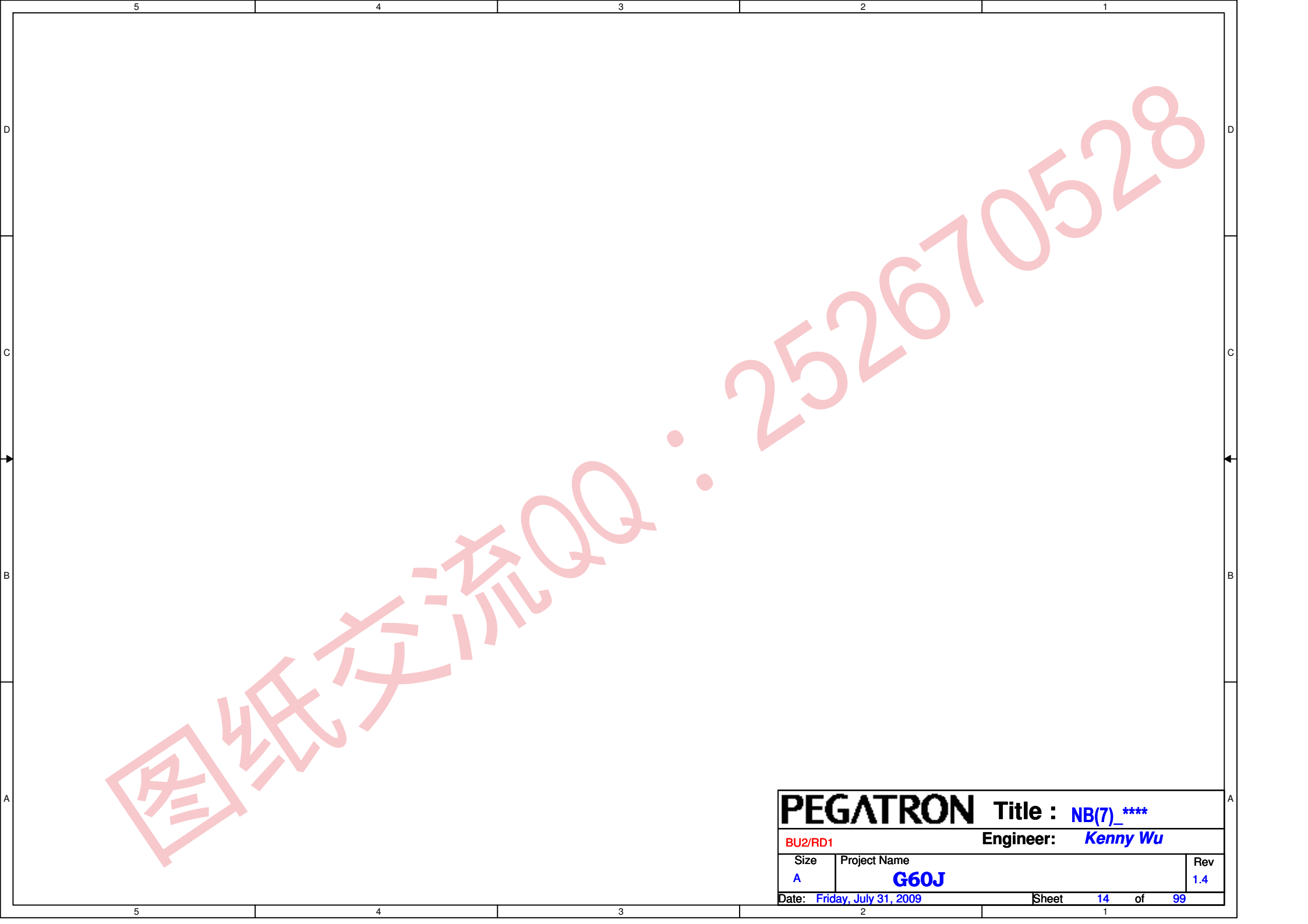
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Custom	<b>G60J</b>		1.4
Date: <b>Friday, July 31, 2009</b>		Sheet	11 of 99

图纸交流QQ : 252670528

<b>PEGATRON</b>		Title : <b>NB(5) ****</b>	
<b>BU2/RD1</b>		Engineer: <b>Kenny Wu</b>	
Size	Project Name		Rev
Custom	<b>G60J</b>		1.4
Date: <b>Friday, July 31, 2009</b>		Sheet	12 of 99

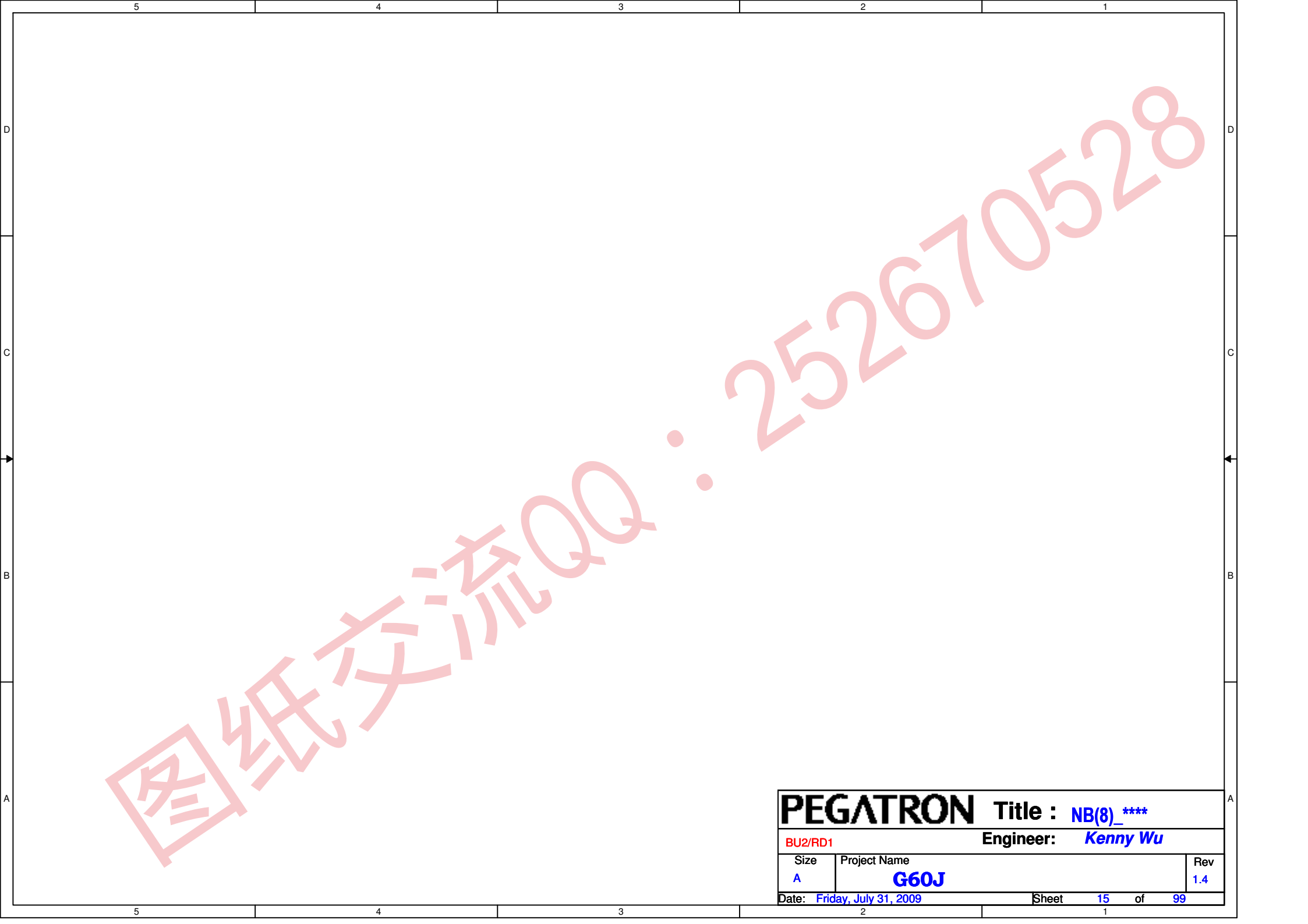
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<b>BU2/RD1</b>		Engineer: <b><i>Kenny Wu</i></b>	
Size	Project Name		Rev
Custom	<b>G60J</b>		1.4
Date: <b>Friday, July 31, 2009</b>		Sheet	13 of 99

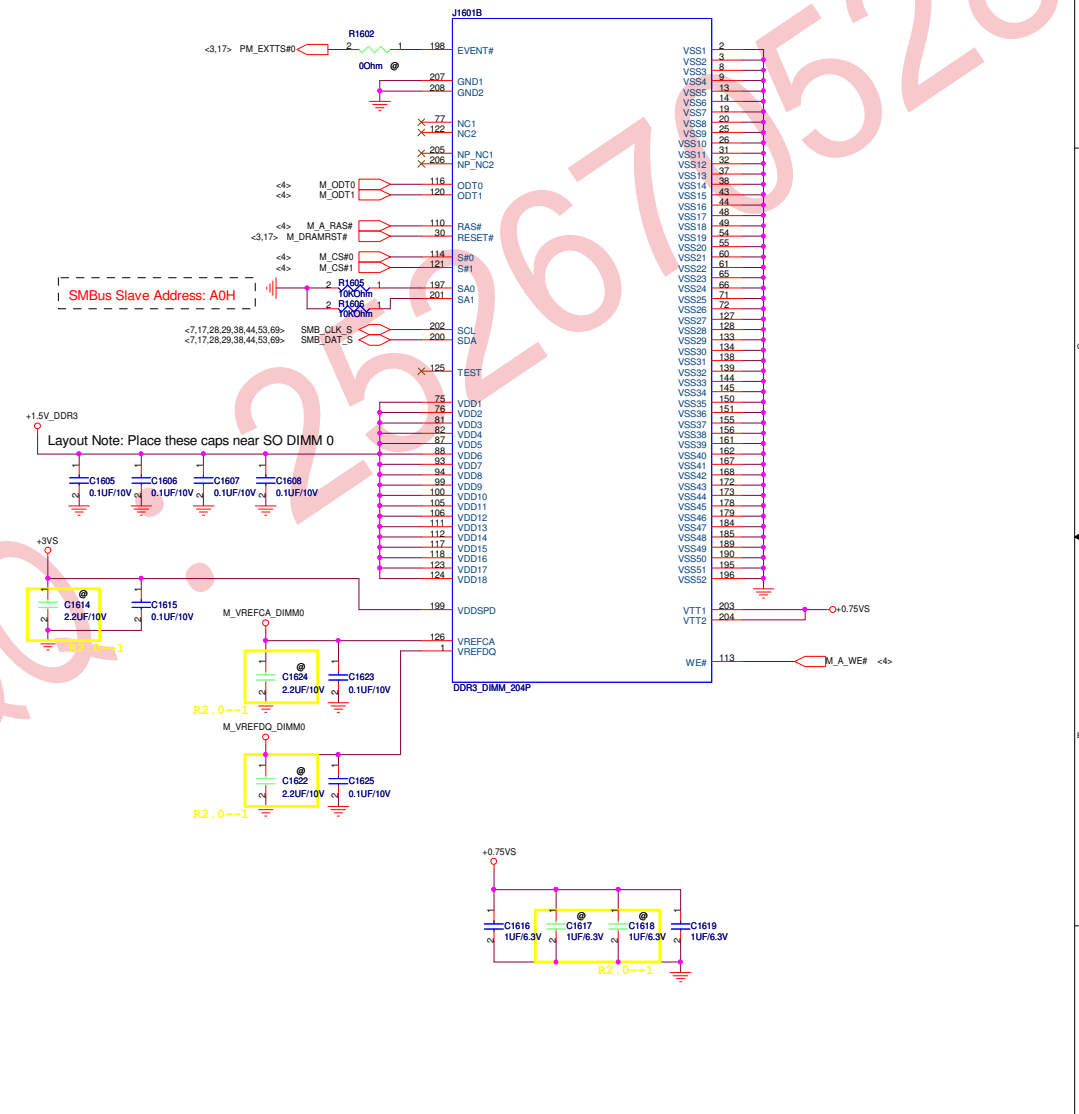
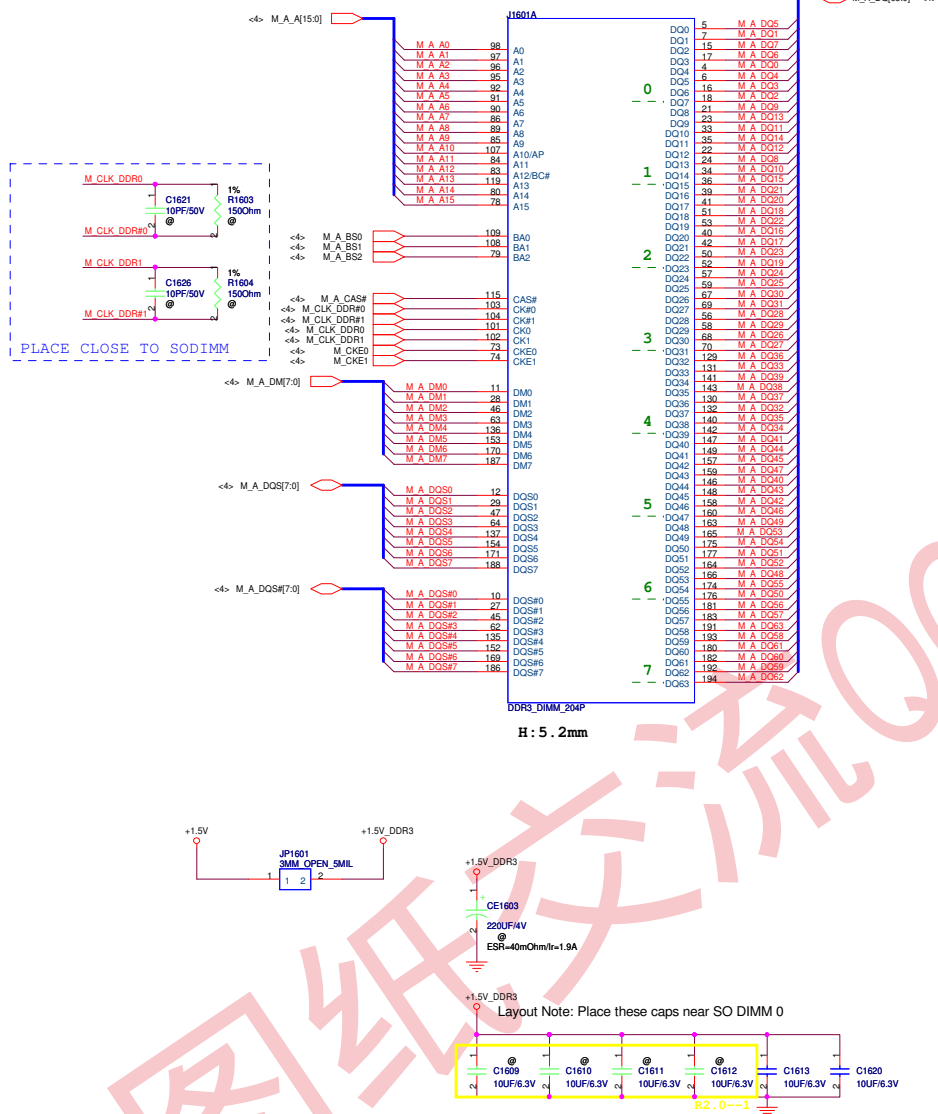


PEGATRON		Title : NB(7) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
A	G60J		1.4
Date: Friday, July 31, 2009		Sheet	14 of 99





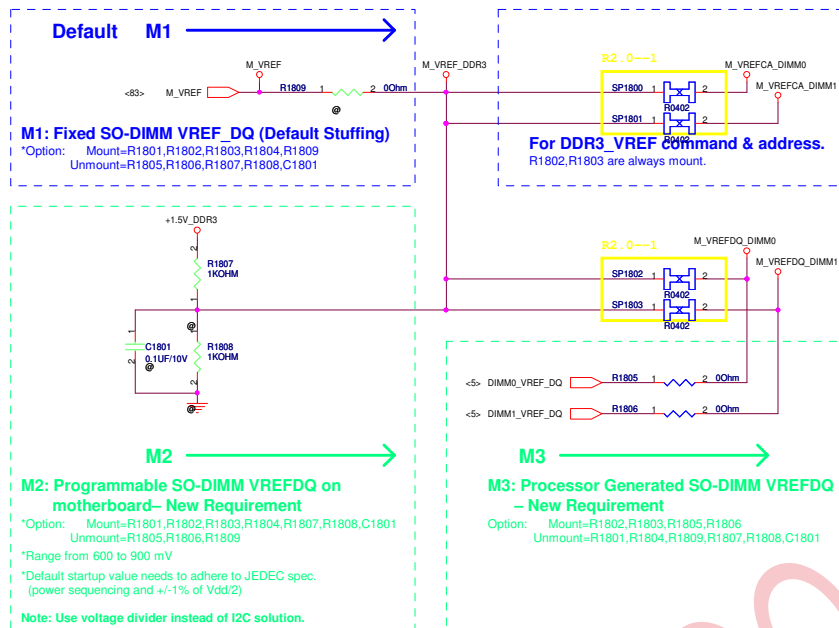
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BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
A	G60J		1.4
Date: Friday, July 31, 2009		Sheet	15 of 99





## DDR3 Vref

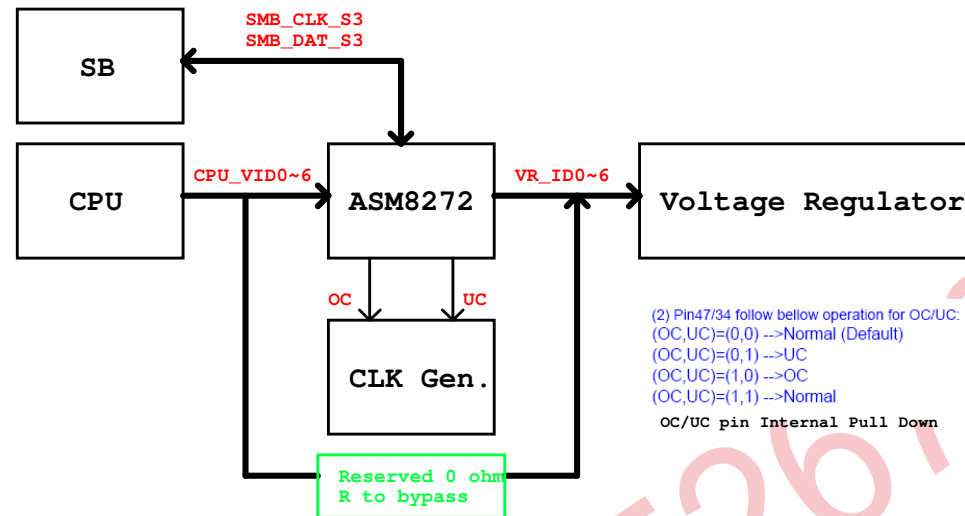
Intel Document Number: 400755  
Calpella Clarksfield DDR3 SO-DIMM VREFDQ  
Platform Design Guide Change Details



+1.5V_DDR3	<16,17>
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+3V0	<24,33,43,45,57,61,64,68,91>
+5VSUS	<27,56,81,91>
+5VA	<31,56,81,82,83>

R1.4--1

# Block Diagram

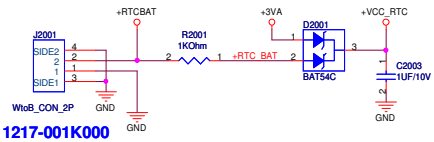


+VTT\_CPU <3,6,7,25,26,27,29,32,57,82>  
+3VS0 <29,48,80,91,92>

CPU_VID6	CPU_VID5	CPU_VID4	CPU_VID3	CPU_VID2	CPU_VID1	CPU_VID0
2	2	2	2	2	2	2
SL1900	SL1901	SL1902	SL1903	SL1904	SL1905	SL1906
VR_VID6	VR_VID5	VR_VID4	VR_VID3	VR_VID2	VR_VID1	VR_VID0
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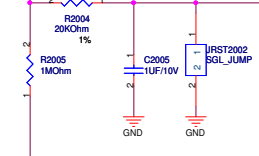
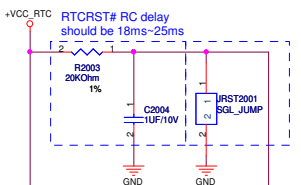
R1.4--2

## RTC battery



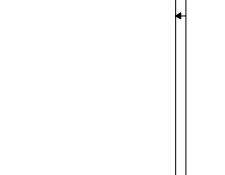
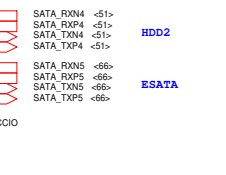
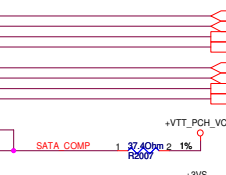
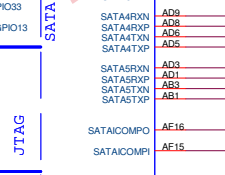
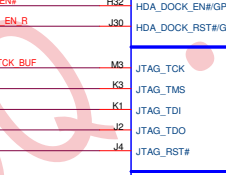
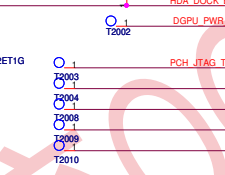
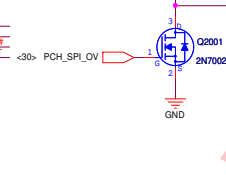
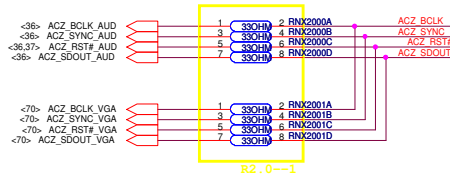
Request by CSC  
for CMOS clear  
function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

HDA\_SYNC: Select VCCVRM 1.5V or 1.8V



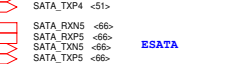
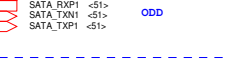
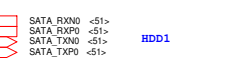
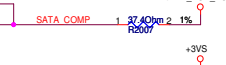
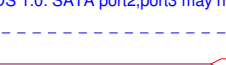
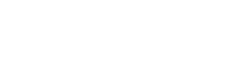
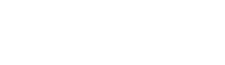
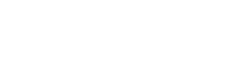
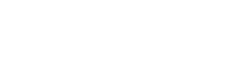
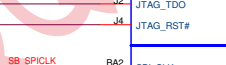
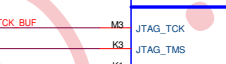
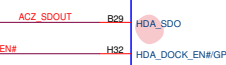
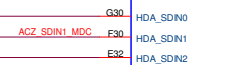
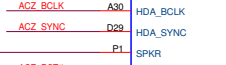
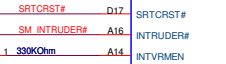
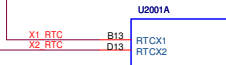
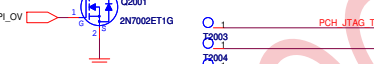
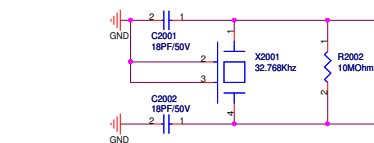
## Strap information:

HDA\_SPKR: No reboot strap  
Low: Disable.  
High: Enable

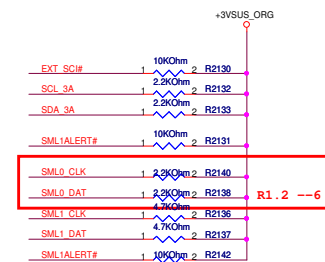
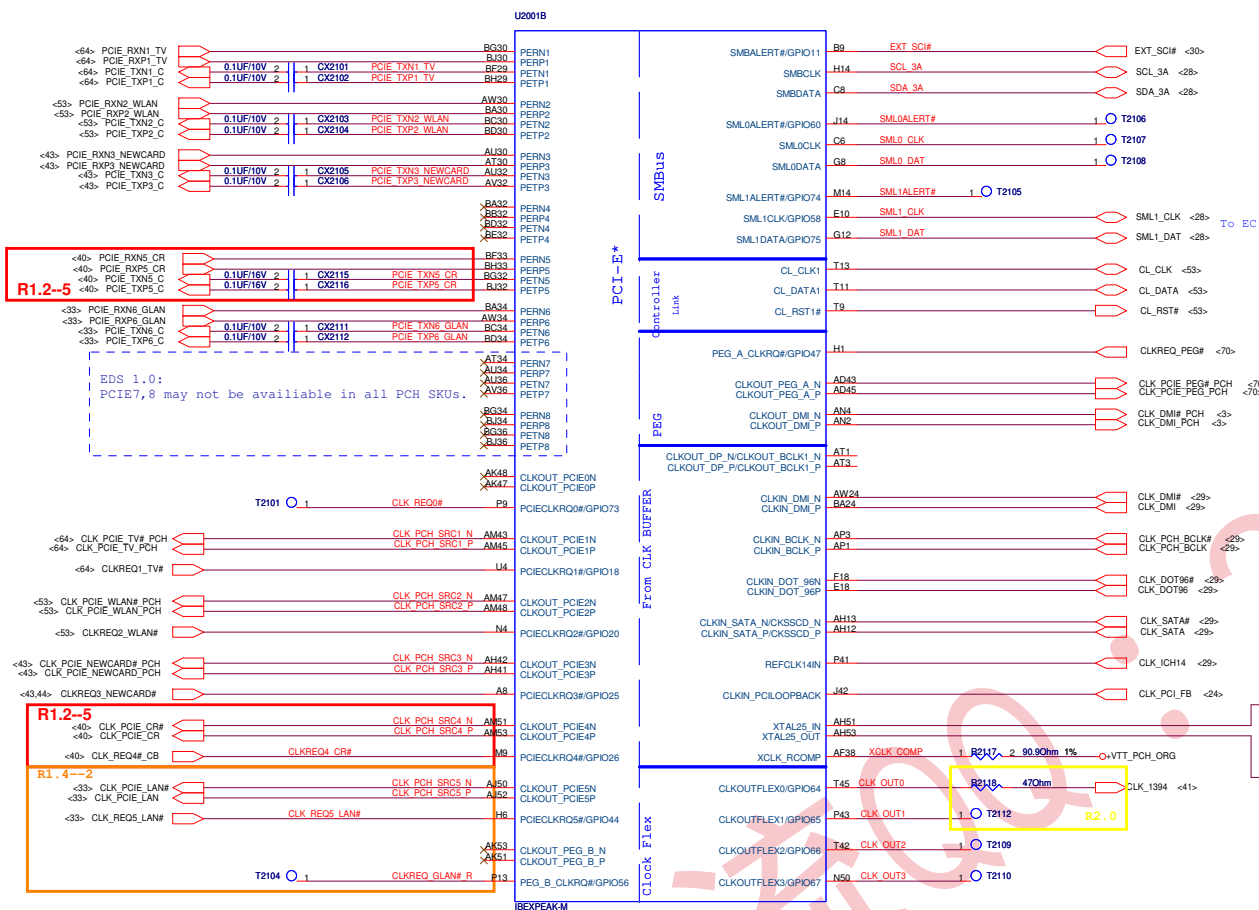
HDA\_DOCK\_EN#:  
1. Flash descriptor security:  
Sampled low: override  
Sampled high: in effect.  
2. GPIO33 low on the rising edge of PWROK,  
Will also disable Intel ME.

SPI\_MOSI: iTPM strap.  
Mount R2015: Enable  
Unmount R2015: Disable (default)

+1.05VS <1.05VS <26,27,57,69,91>  
+VCC\_RTC <VCC\_RTC <27>  
+3VS <3VS <29,48,80,91,92>  
+1.05VM\_ORG <1.05VM\_ORG <27>  
+VTT\_PCH\_VCCIO <VTT\_PCH\_VCCIO <26,27>  
+3VM\_SPI <3VM\_SPI <28>

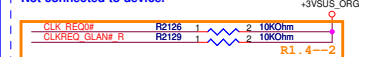






### PCH CLKREQ Setting:

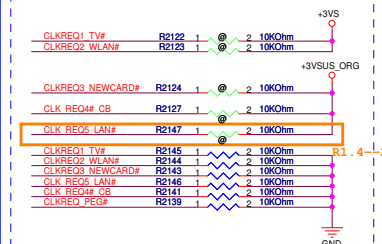
Not connected to device.

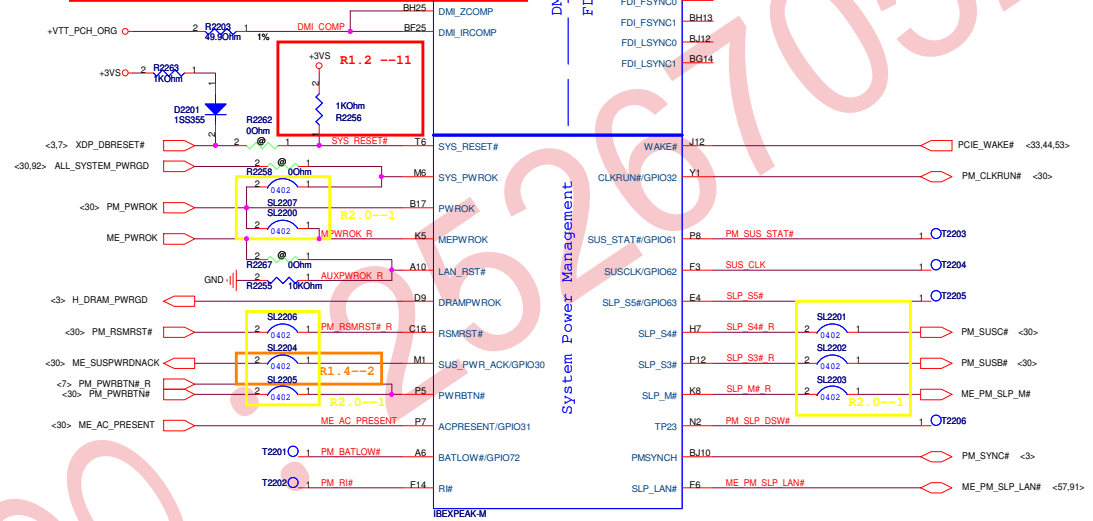
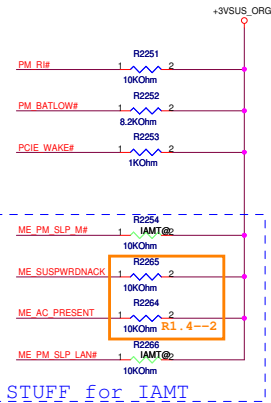


Connected to device.

Default : Clock free run. (PD 10K).

- Reserver 10K PU for power saving purpose.

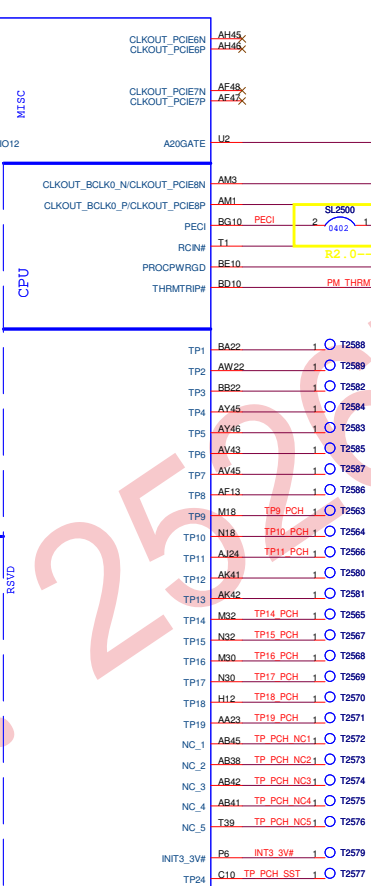
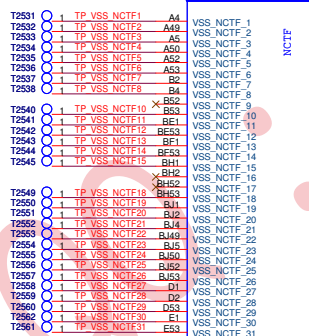
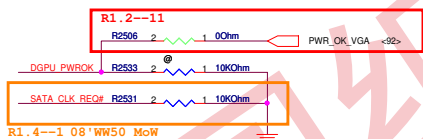


[illegible]

+3VSUS\_ORG  +3VSUS\_ORG <21,24,25,27>  
+3VS  +3VS <29,48,80,91,92>  
+VTT\_PCH\_ORG  +VTT\_PCH\_ORG <21,26,27>

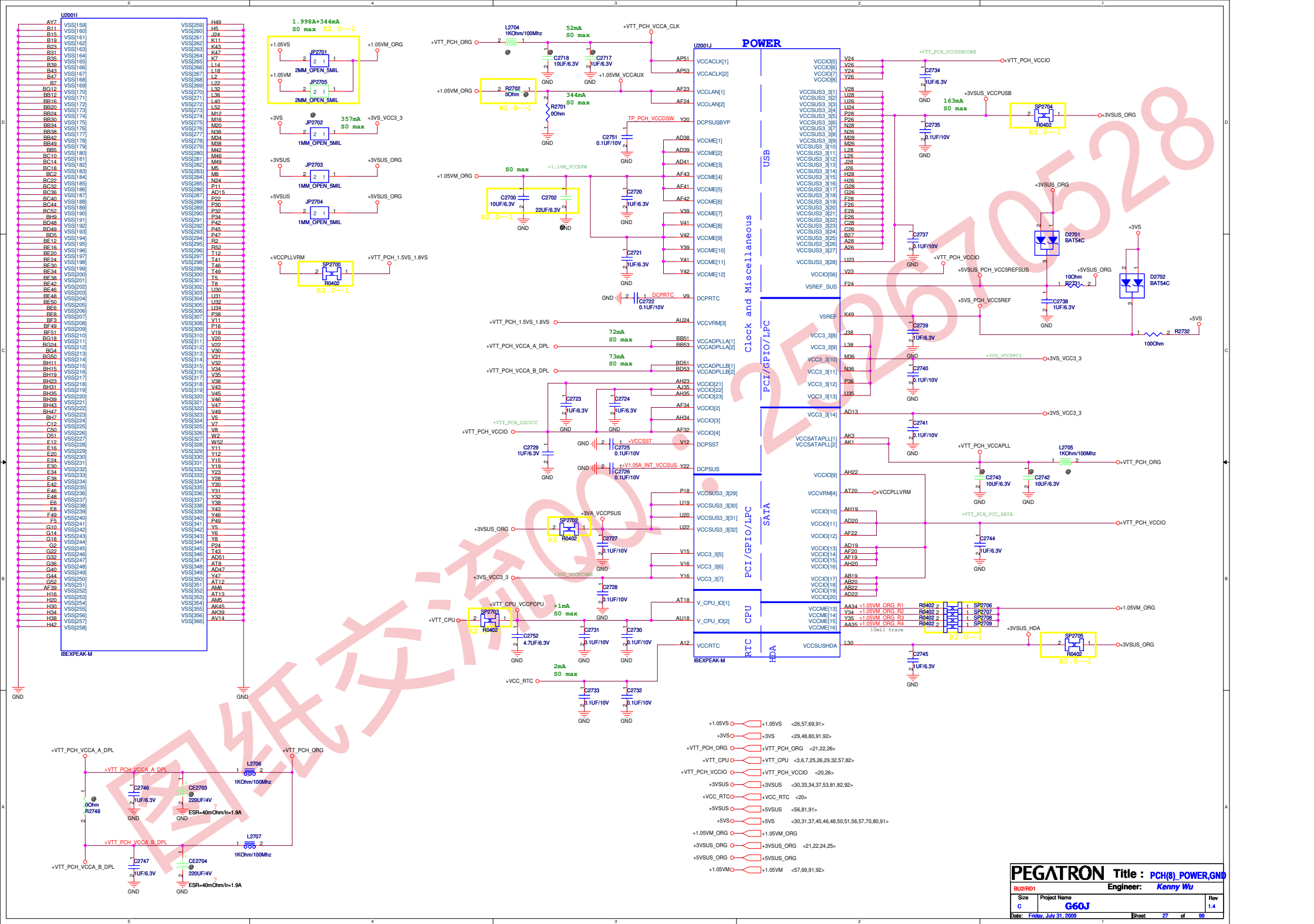




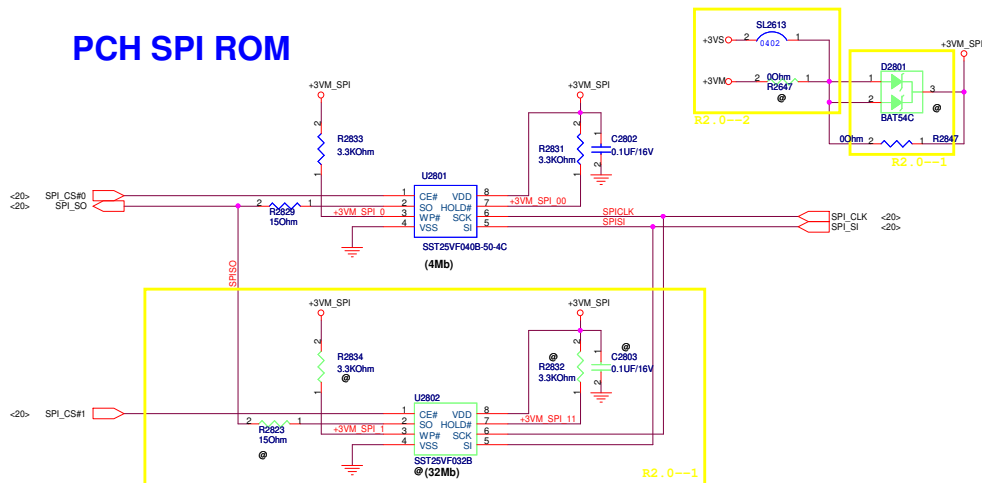








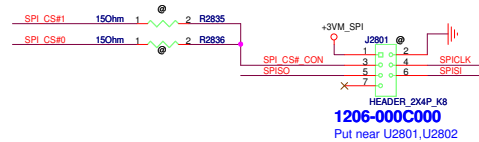
## PCH SPI ROM



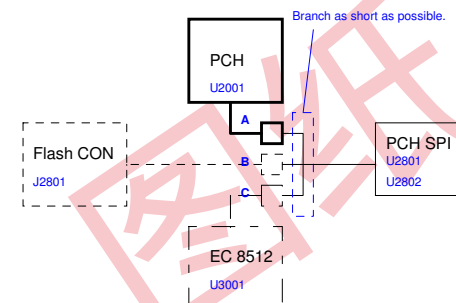
## SPI FROM EC

For EC request.

## SPI FLASH CON



## SPI Setting for layout:

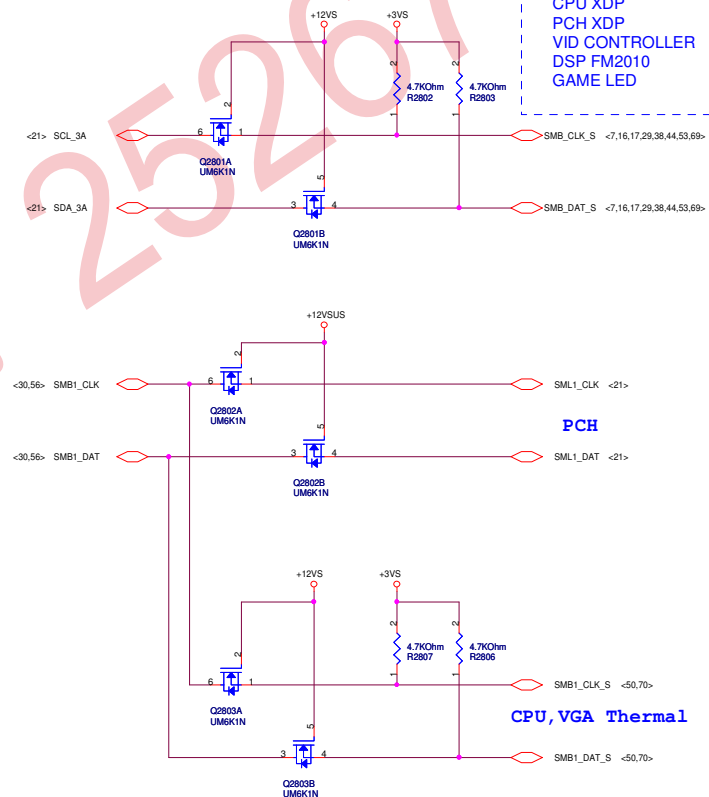


PCH

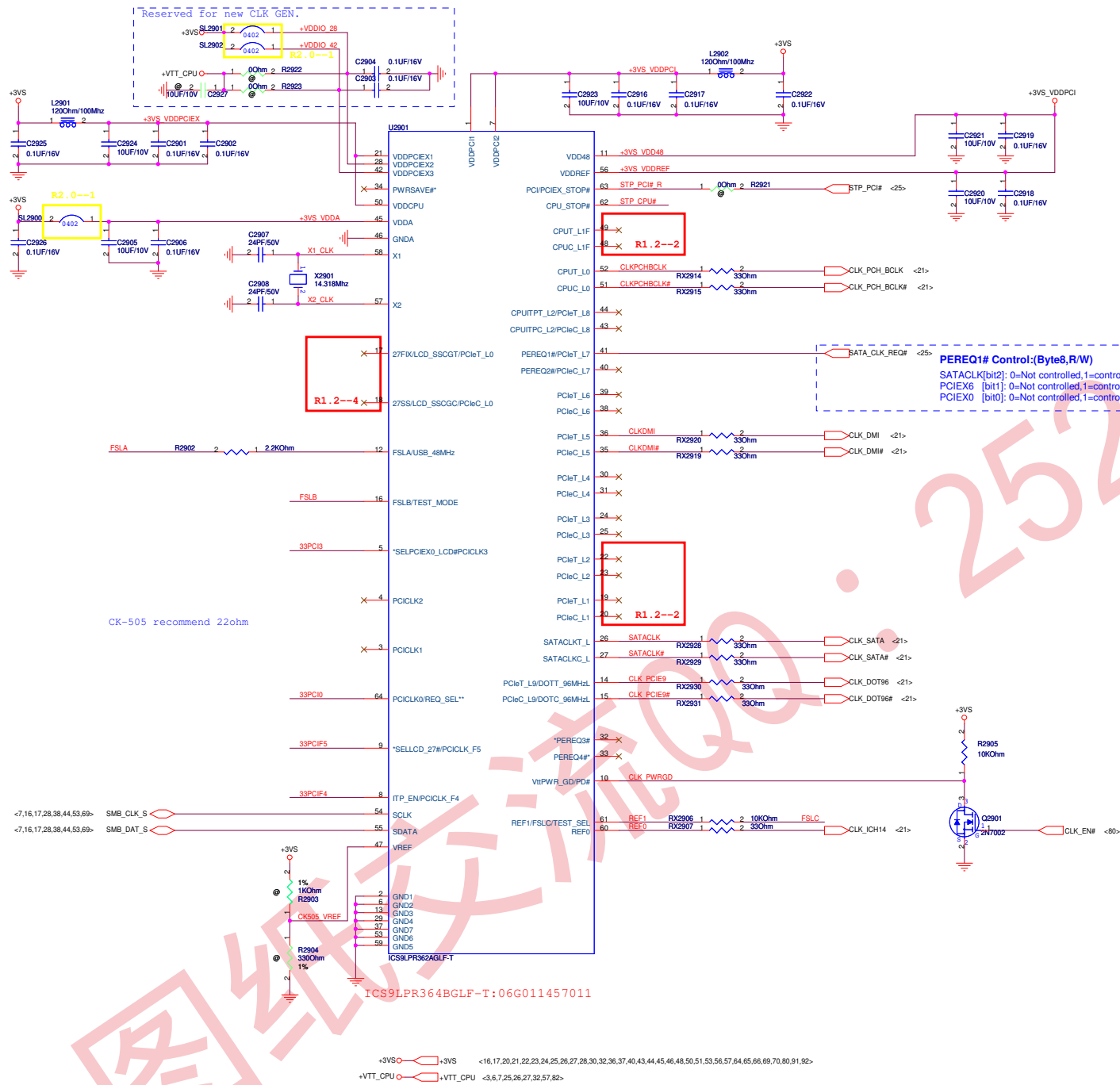
EC

+3VS <16,17,20,21,22,23,24,25,26,27,29,30,32,36,37,40,43,44,45,46,48,50,51,53,56,57,64,65,66,69,70,80,91,92>  
 +12VS <45,91>  
 +12VSUS <81,91>  
 +3VM <26,53,57,91,92>  
 +3VM\_SPI <20>

SMBUS Link device  
 SPD  
 CLKGEN  
 DEBUG  
 WLAN  
 CPU XDP  
 PCH XDP  
 VID CONTROLLER  
 DSP FM2010  
 GAME LED



CPU,VGA Thermal



## Latched Input Select

Pin5 desides pin17/18:

0 : Pin 17/18 = LCD\_SSCG

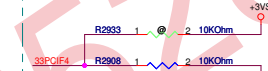
1 : Pin 17/18 = PCIe\_L0



Pin8 desides pin43/44:

0 : Pin 43/44 = SRC CLK

1 : Pin 43/44 = CPU\_ITP CLK



Pin9 desides pin14/15,17/18:

0 : Pin 14/15 = PCIe\_L9

Pin 17/18 = 27FIX/27SS

1 : Pin 14/15 = DOT\_96MHz

Pin 17/18 = LCD\_SSCG/PCIe\_L0



Pin64 desides pin40/41:

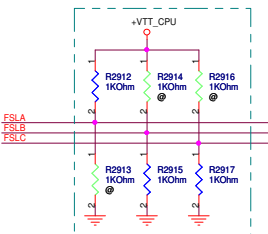
0 : Pin 40/41 = PCIe\_L7

1 : Pin 40/41 = PEREQ1#,PEREQ2#



Reserved for R1.0 Debug

BCLK	FSB	FSLC	FSLB	FSLA
133	0	0	1	1
166	0	1	1	1
200	0	1	0	0
266	0	0	0	0



	R2903	R2904	R2925
363:VREF	1K	330	0
364:TURBO	0	10K	0
364:NO TURBO	0	0	0

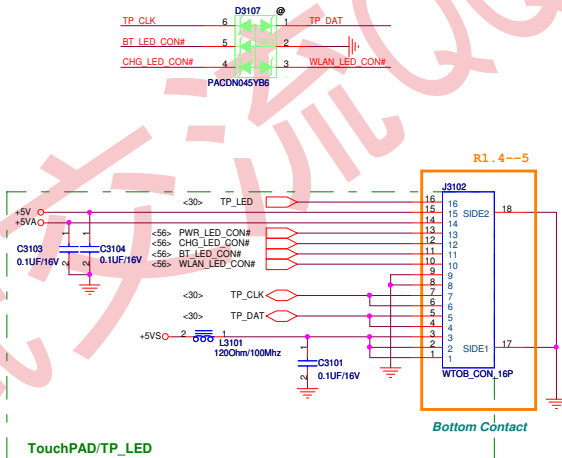
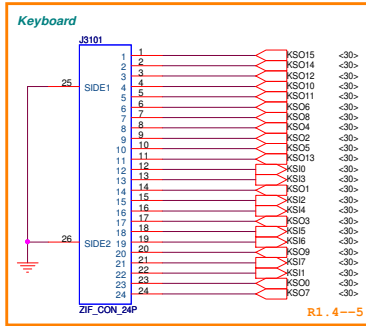
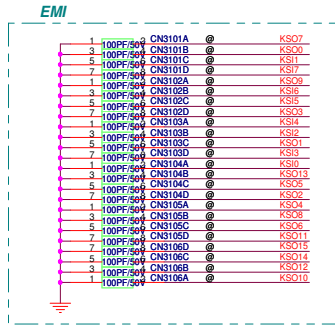
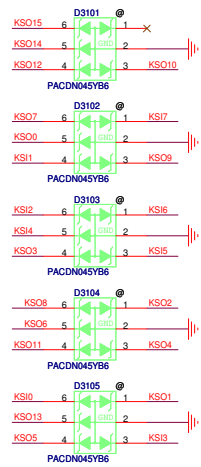
PEGATRON Title : CLK\_IC9LPR362

BU2RD1 Engineer: Gary Tsai

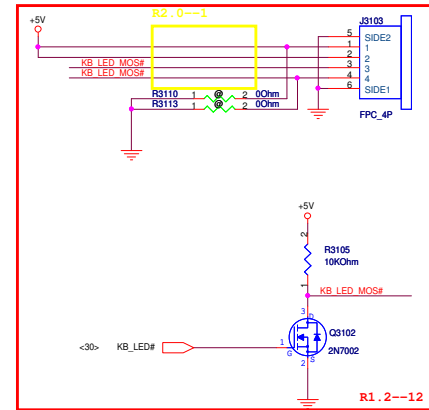
Size Project Name G50J Rev 1.2

Date: Friday, July 31, 2009 Sheet 29 of 99

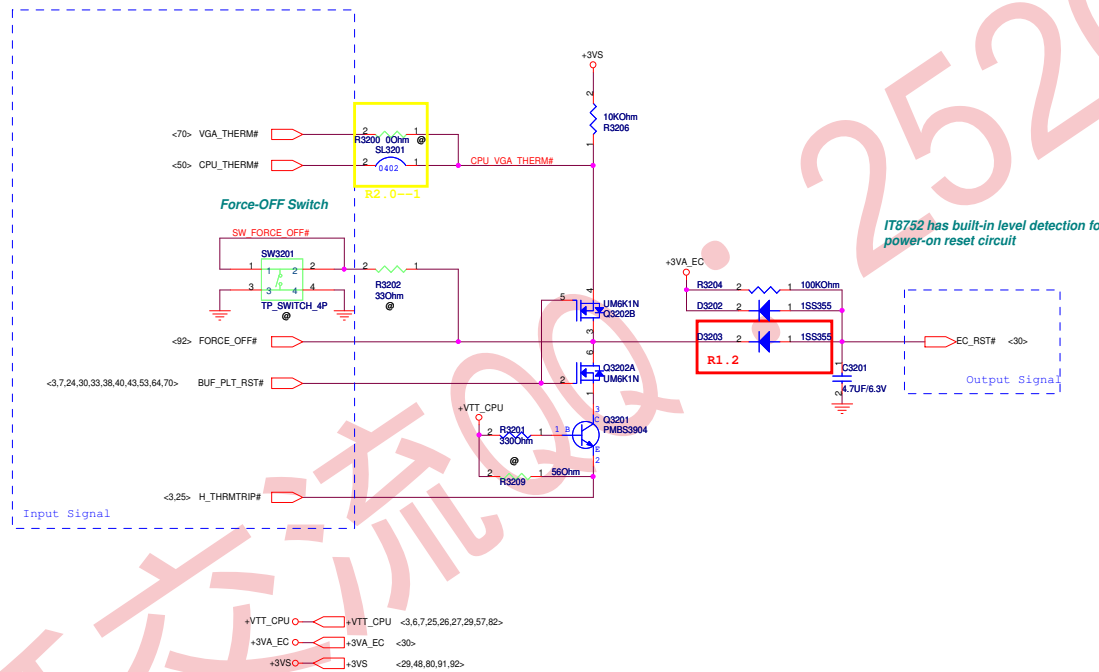




+3VA_EC	+3VA_EC	<30,32>
+3VO	+3V	<24,33,43,45,57,61,64,69,91>
+3VS	+3VS	<29,48,80,91,92>
+5VA	+5VA	<56,81,82,83>
+5VO	+5V	<36,44,45,52,56,57,65,69,91>
+5VS	+5VS	<27,30,37,46,48,50,51,56,57,70,80,91>

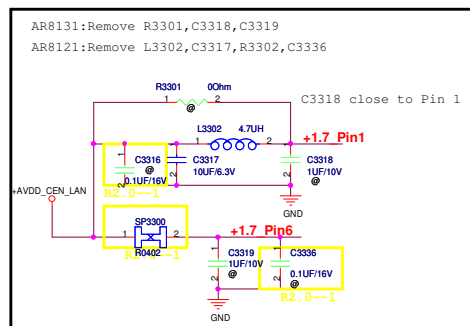


# Thermal Policy





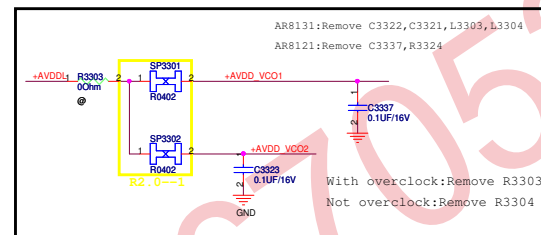
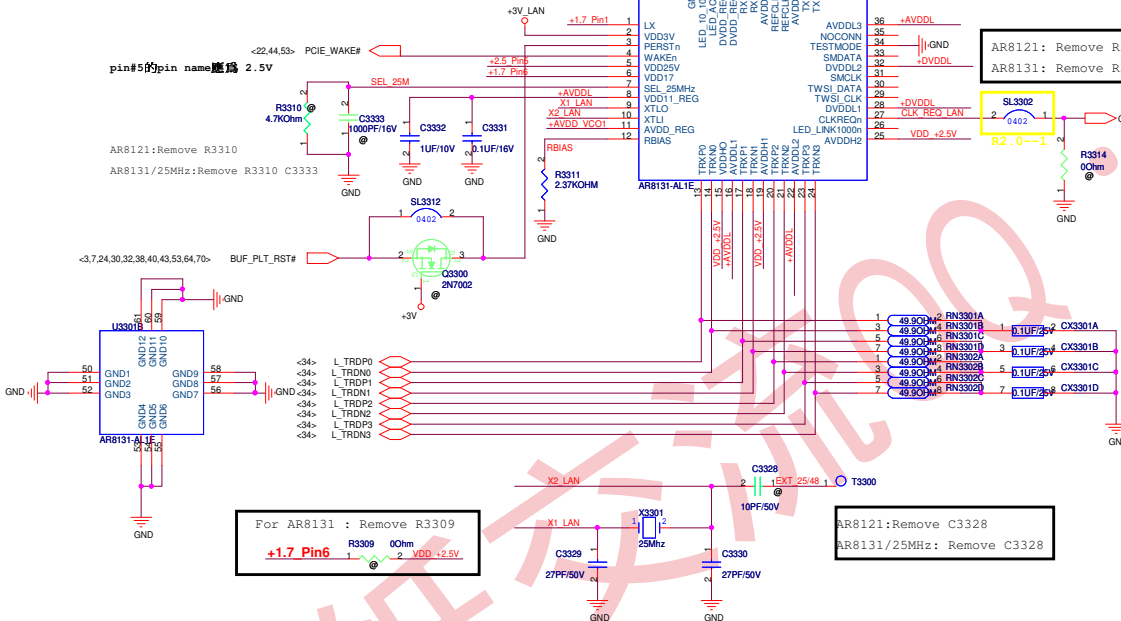
+3VS  +3VS <29,48,80,91,92>  
+3VSUS  +3VSUS <27,30,34,37,53,81,82,92>



```
AR8131 with overclock: Remove R3315
AR8121:Remove R3315
```

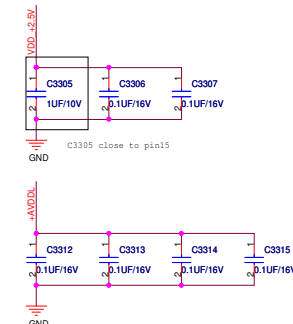
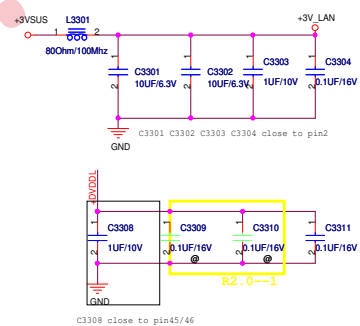
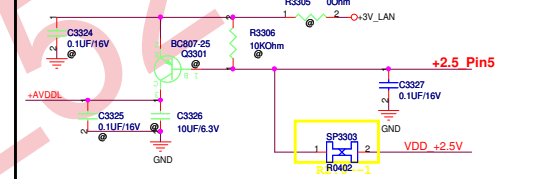
ground pad要打散熱孔

PCIE Tx,Rx方向是以南橋為觀點
Chip pin Tx,Rx是以chip為觀點



With overclock:Remove R3303  
Not overclock:Remove R3304

```
For AR8131: Remove R3305,R3306,C3324,C3325,C3326,Q3301
For AR8121: Remove C3327 R3308
Q3301 close to Pin8
```

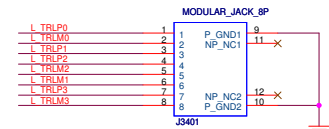
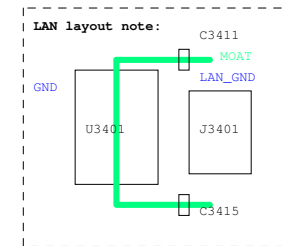
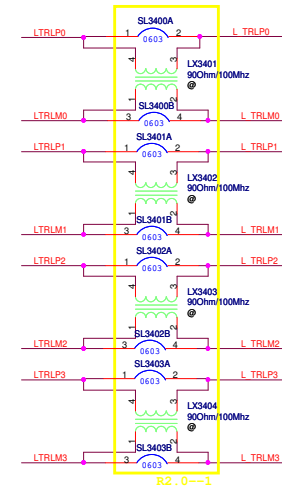
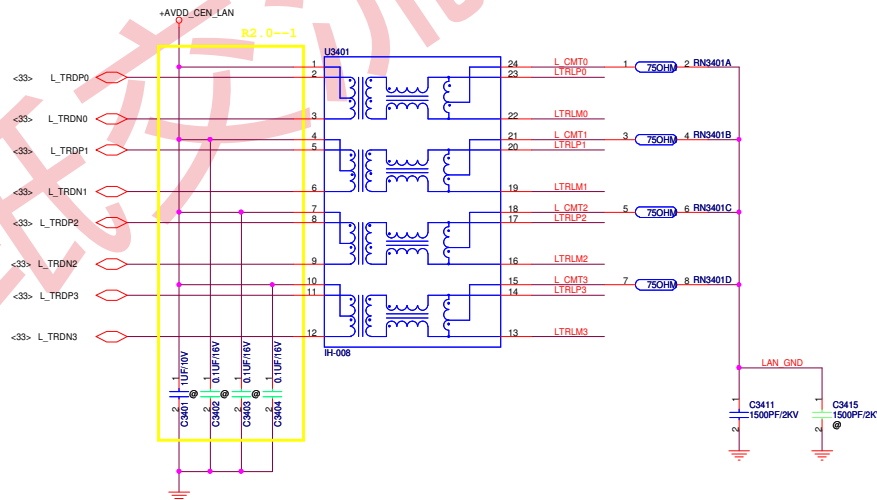
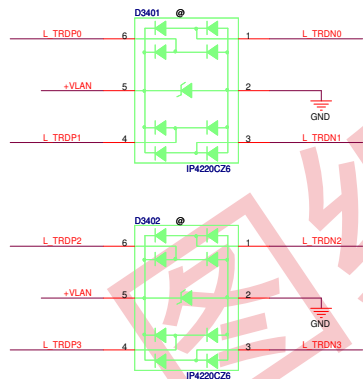
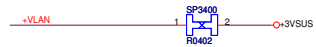


R1.4--3

STUFF for NON\_IAMT

STUFF for IAMT

R1.4-2

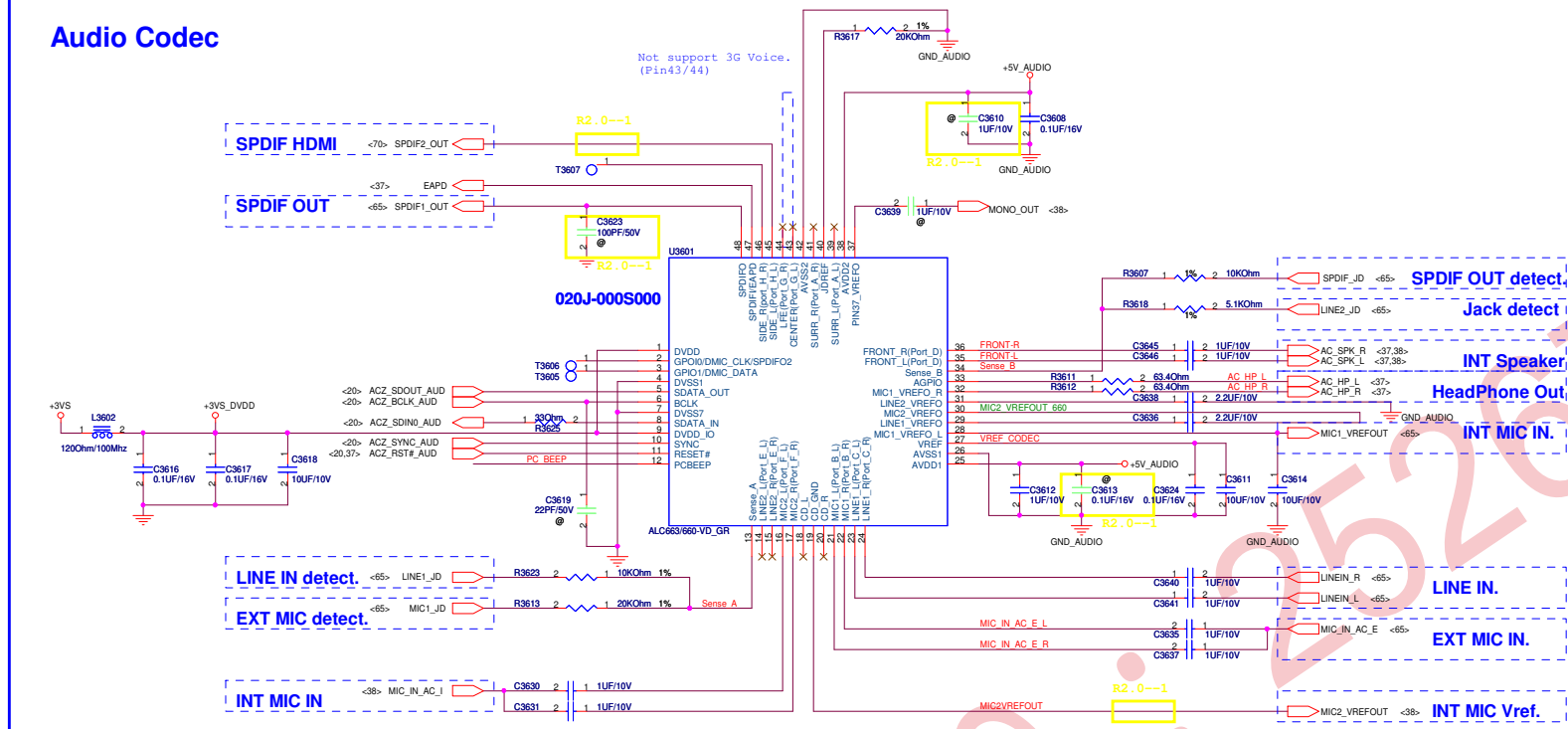


图纸交流QQ : 252670528

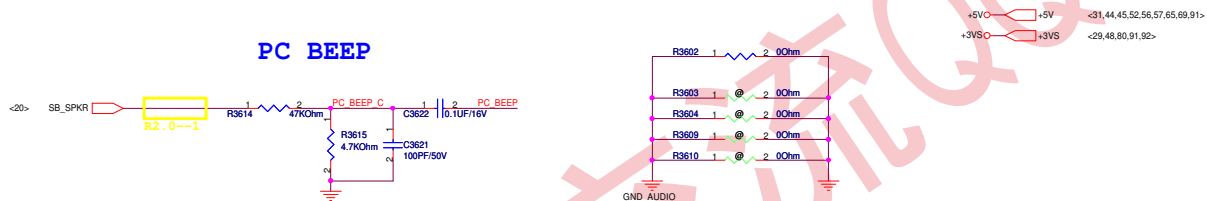
PEGATRON		Title : MDC_****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	35 of 99

## Audio Codec

Not support 3G Voice.  
(Pin43/44)



## PC BEEP



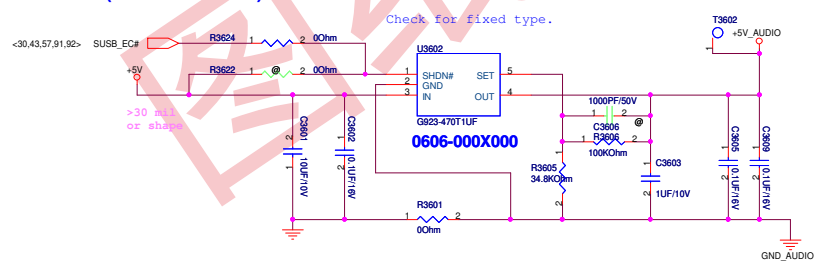
## Audio Power

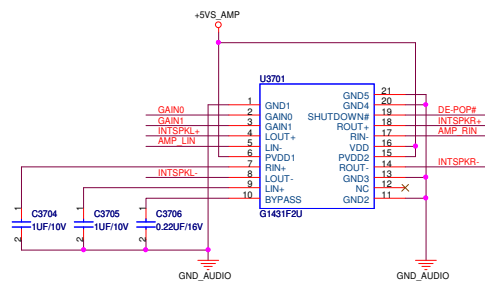
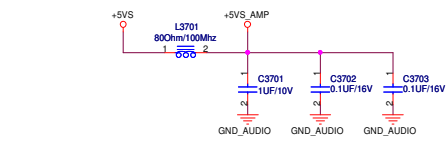
FOR ADJUST MODE:

$$V_o = 1.25 \times (1 + R_{3706}/R_{3705})$$

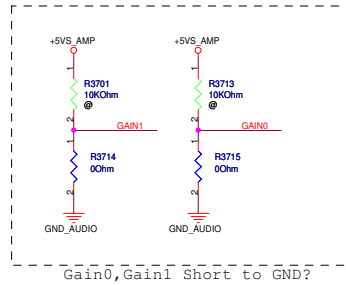
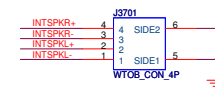
$$= 1.25 \times (1 + 100K/34.8K) = 4.84$$

Check for fixed type.

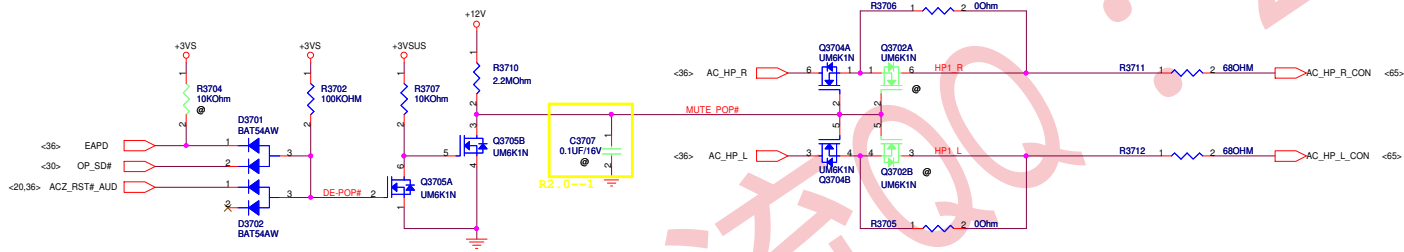
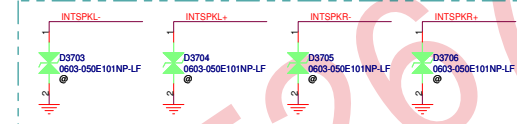




Internal Speaker Conn.



Reserved for EMI



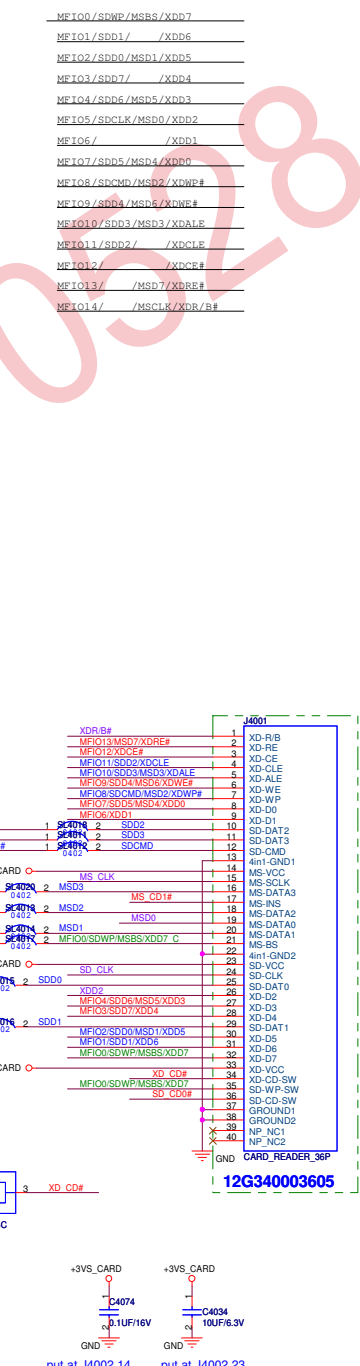
- +5VS <27,30,31,45,46,48,50,51,56,57,70,80,91>
- +3VSUS <27,30,33,34,53,81,82,92>
- +12V <91>
- +3VS <29,48,80,91,92>



图纸交流QQ : 252670528

PEGATRON		Title : AUD(4) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet	39	of 99

R1.2,item L1





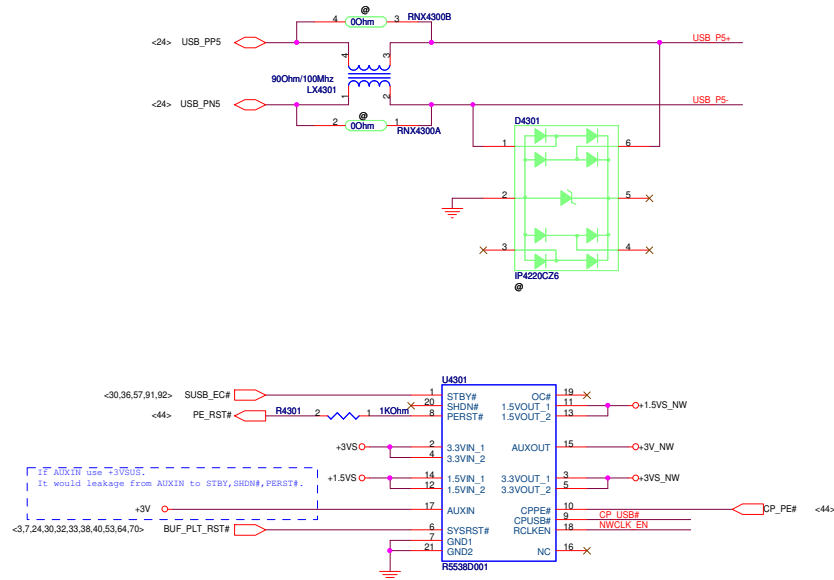
+3VS O  +3VS <29.48,80.91.92>

图纸交流QQ : 252670528

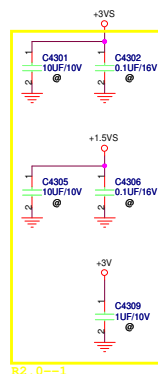
PEGATRON		Title : CB(2)_R5C833	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	41 of 99

+3VS  +3VS <29,48,80,91,92>  
+12V  +12V <37,91>

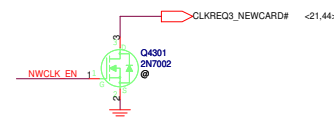
图纸交流QQ: 252670528



+1.5VS  $\rightarrow$  +1.5VS <26,53,57,64,91>  
 +3V  $\rightarrow$  +3V <24,33,45,57,61,64,69,91>  
 +3VS  $\rightarrow$  +3VS <29,48,80,91,92>



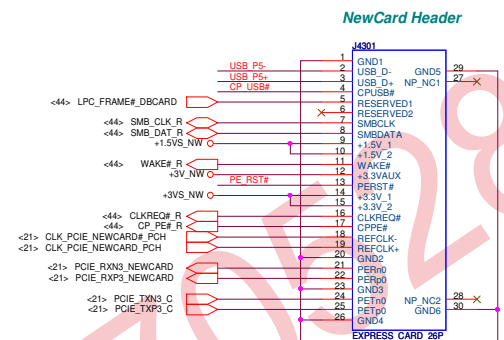
R2\_0--1



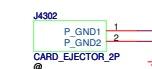
3.0V-3.6V  
 Ave= 1000mA  
 Max= 1300 mA

1.35V-1.65V  
 Ave= 500 mA  
 Max= 650 mA

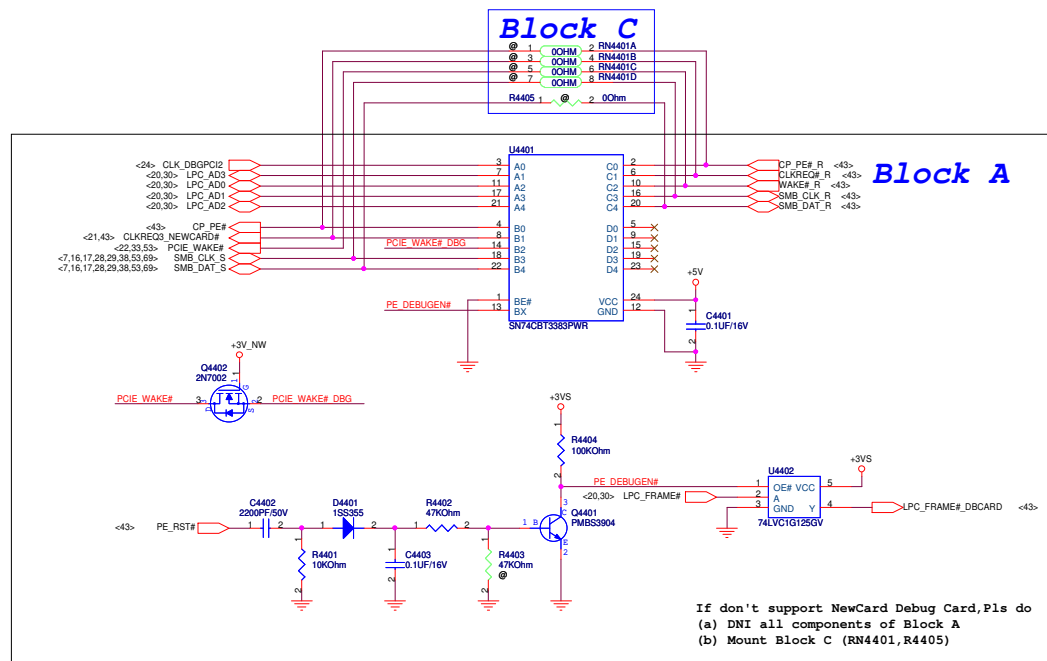
3.0V-3.6V  
 Ave= 200mA  
 Max= 275 mA

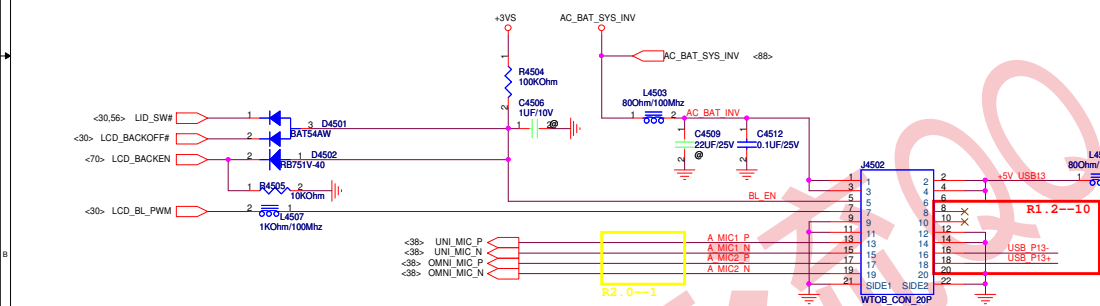
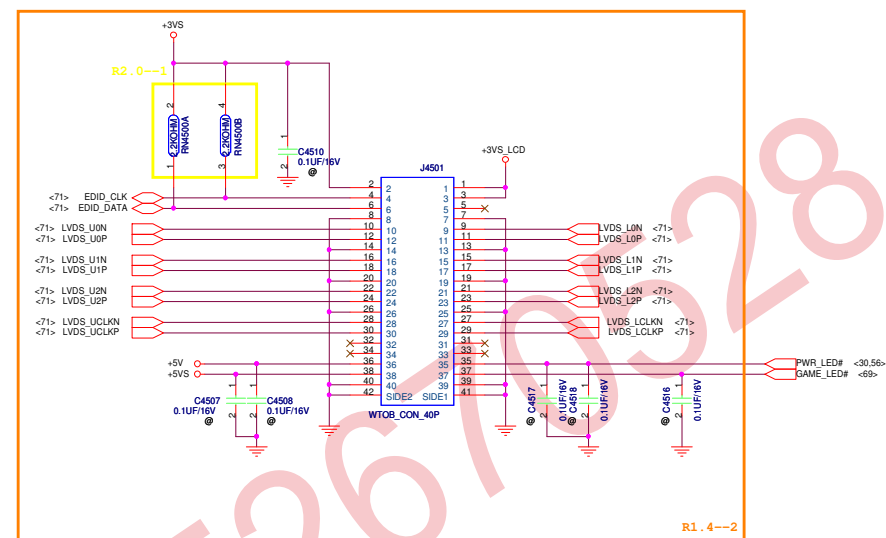
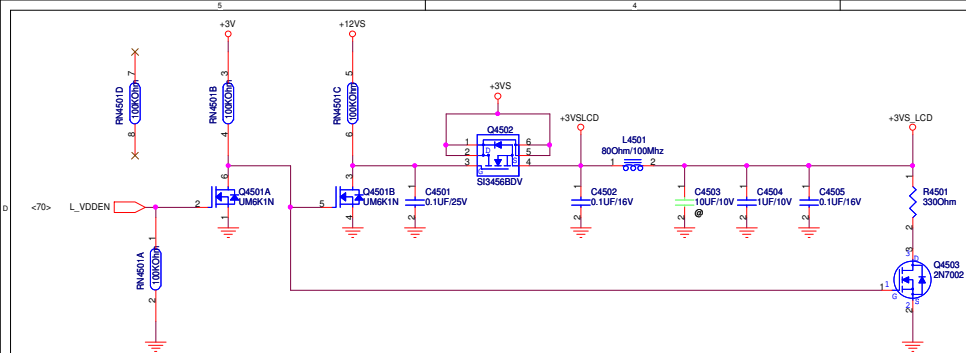


### NewCard Ejector

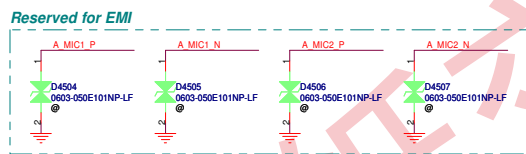
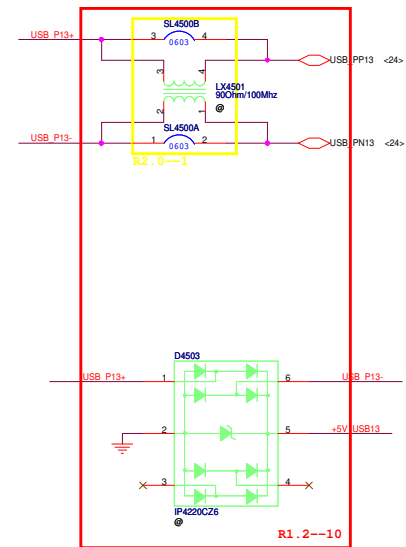


# For NewCard Debug Card

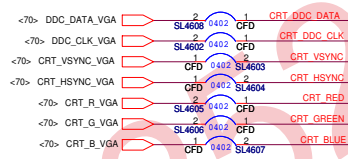
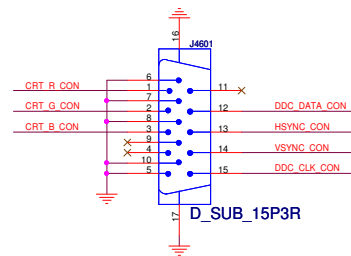
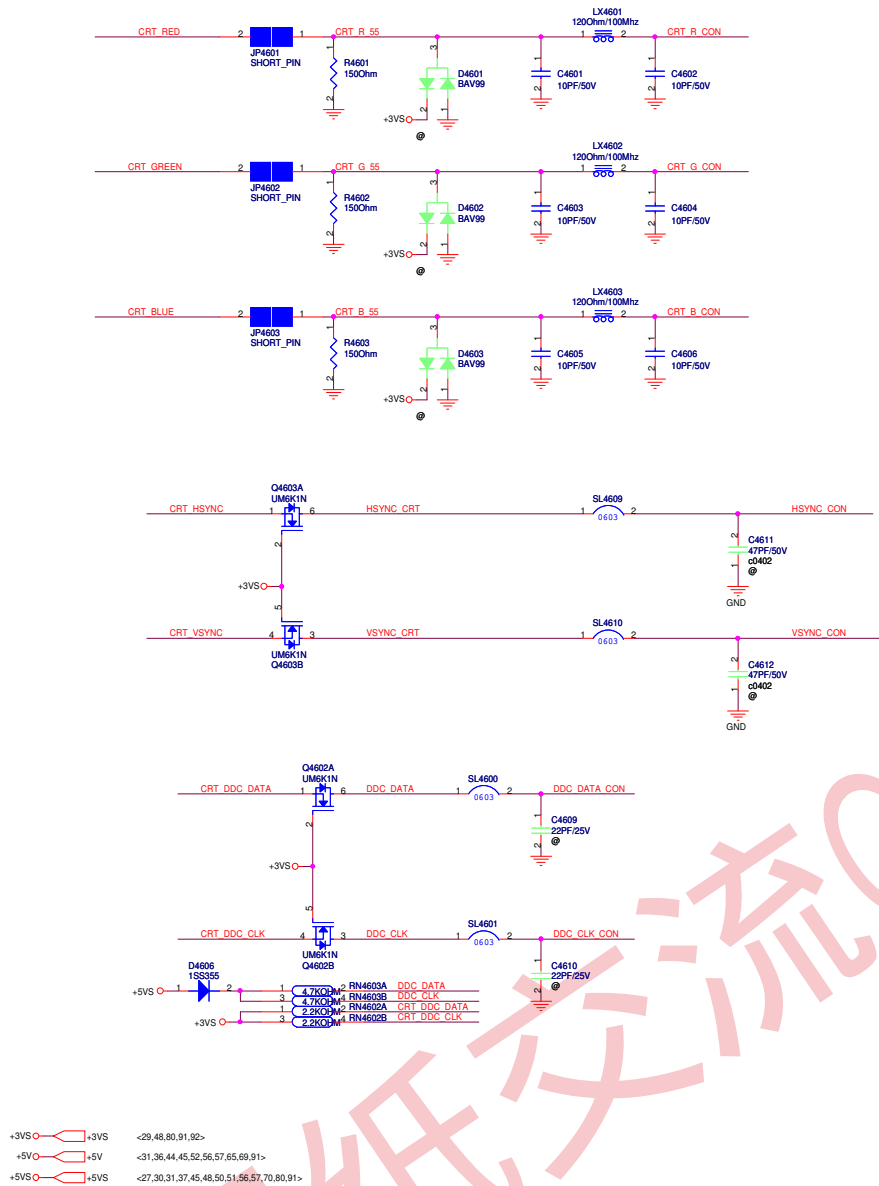






This setting is for M52J/G50J colay:  
M52J: Camera\*1 (F4501, L4502 can cost down)  
G50J: USB portx1, Camerax1.



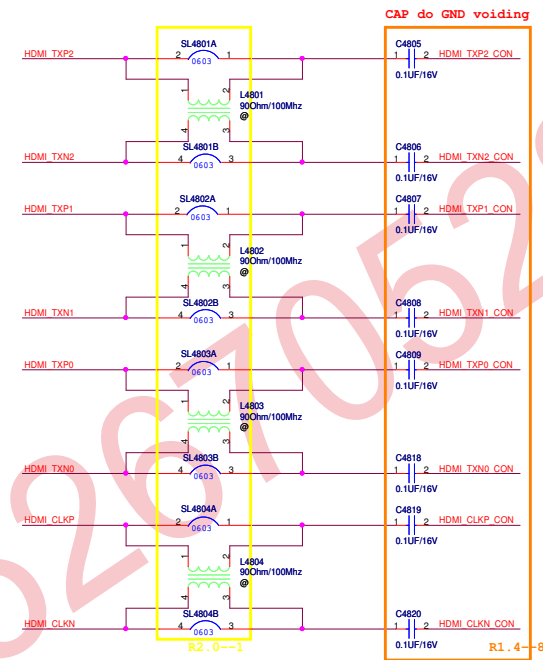
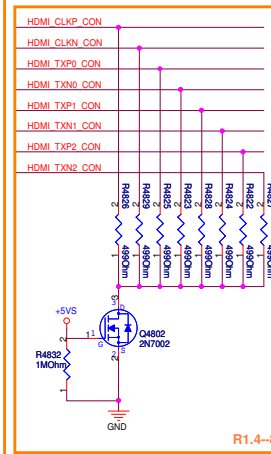
- +3VS -> +3VS <29,48,80,91,92>
- +3V -> +3V <24,33,43,57,61,64,69,91>
- +12VS -> +12VS <28,91>
- +5V -> +5V <31,36,44,52,56,57,65,69,91>
- +5VS -> +5VS <27,30,31,37,46,48,50,51,56,57,70,80,91>





+3VS  +3VS      <29,48,80,91,92>  
+5VS  +5VS      <27,30,31,37,45,46,48,50,51,56,57,70,80,91>

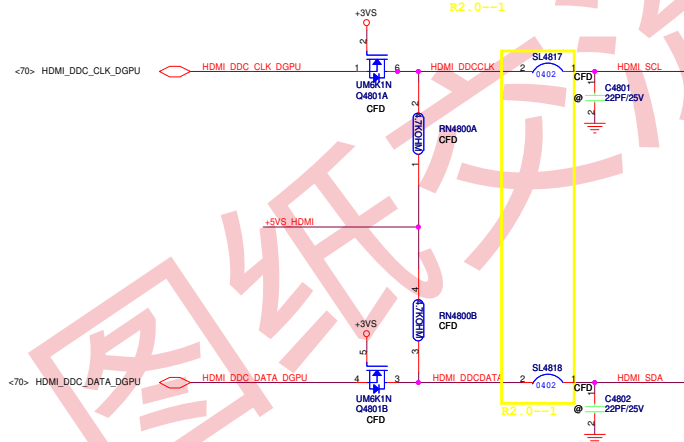
R2.0



CFD

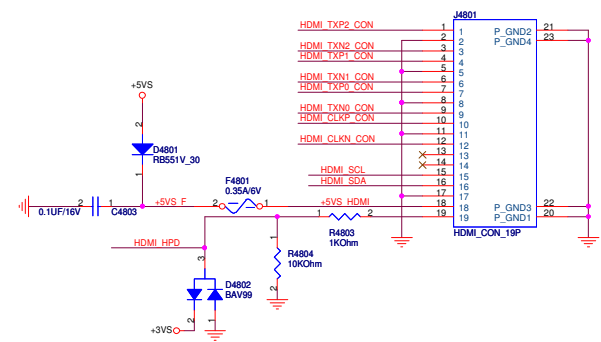
- <70> HDMI\_HPD\_DGPU SL4800 2 1 HDMI\_HPD
- <70> HDMI\_CLKN\_DGPU CFD1 2 2 RN4805A HDMI\_CLKN
- <70> HDMI\_CLKP\_DGPU CFD3 2 2 RN4805A HDMI\_CLKP
- <70> HDMI\_TXN0\_DGPU CFD1 2 2 RN4806A HDMI\_TXN0
- <70> HDMI\_TXP0\_DGPU CFD3 2 2 RN4806A HDMI\_TXP0
- <70> HDMI\_TXN1\_DGPU CFD1 2 2 RN4807A HDMI\_TXN1
- <70> HDMI\_TXP1\_DGPU CFD3 2 2 RN4807A HDMI\_TXP1
- <70> HDMI\_TXN2\_DGPU CFD1 2 2 RN4808A HDMI\_TXN2
- <70> HDMI\_TXP2\_DGPU CFD3 2 2 RN4808A HDMI\_TXP2

R2.0-1



R1.4-7

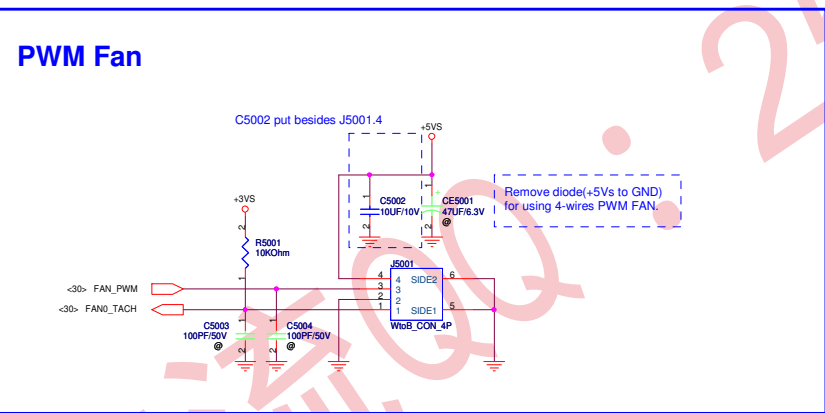
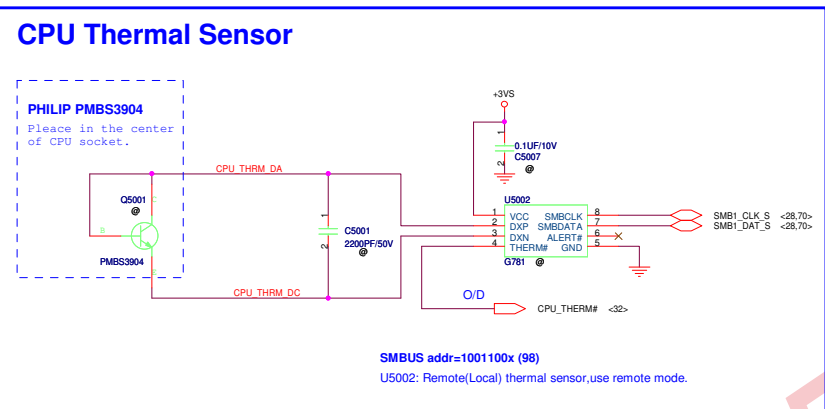
- <70> HDMI\_HPD\_DGPU SL4800 2 1 HDMI\_HPD
- <70> HDMI\_CLKN\_DGPU CFD1 2 2 RN4805A HDMI\_CLKN
- <70> HDMI\_CLKP\_DGPU CFD3 2 2 RN4805A HDMI\_CLKP
- <70> HDMI\_TXN0\_DGPU CFD1 2 2 RN4806A HDMI\_TXN0
- <70> HDMI\_TXP0\_DGPU CFD3 2 2 RN4806A HDMI\_TXP0
- <70> HDMI\_TXN1\_DGPU CFD1 2 2 RN4807A HDMI\_TXN1
- <70> HDMI\_TXP1\_DGPU CFD3 2 2 RN4807A HDMI\_TXP1
- <70> HDMI\_TXN2\_DGPU CFD1 2 2 RN4808A HDMI\_TXN2
- <70> HDMI\_TXP2\_DGPU CFD3 2 2 RN4808A HDMI\_TXP2



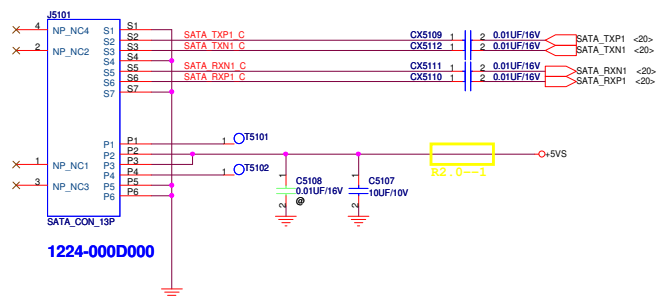


图纸交流QQ : 252670528

PEGATRON		Title : TV(2) ****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	49 of 99

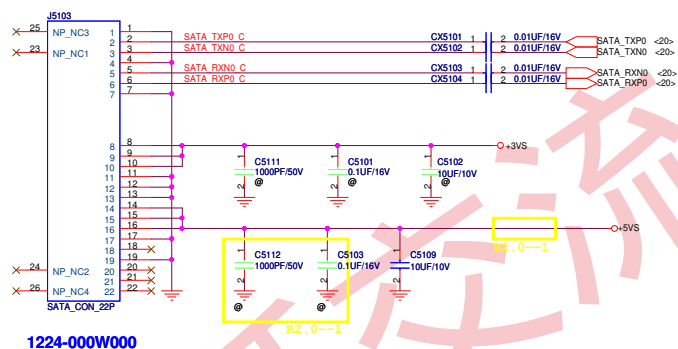


# ODD

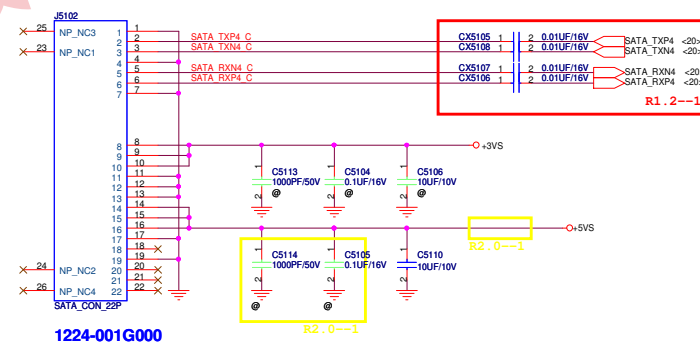


+3VS → +3VS <29,48,80,91,92>  
+5VS → +5VS <27,30,31,37,45,46,48,50,56,57,70,80,91>

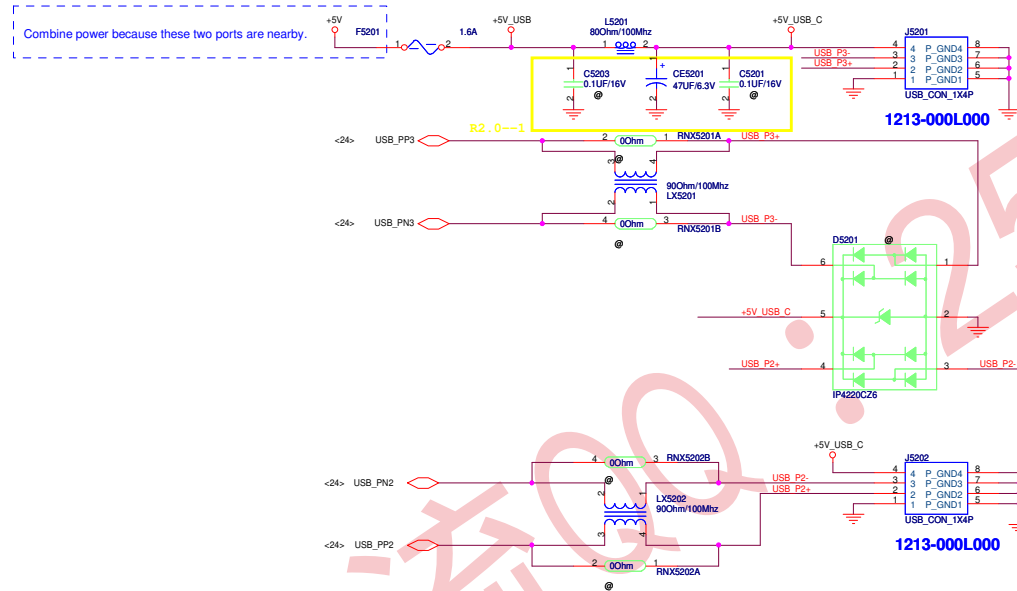
# HDD (1st)

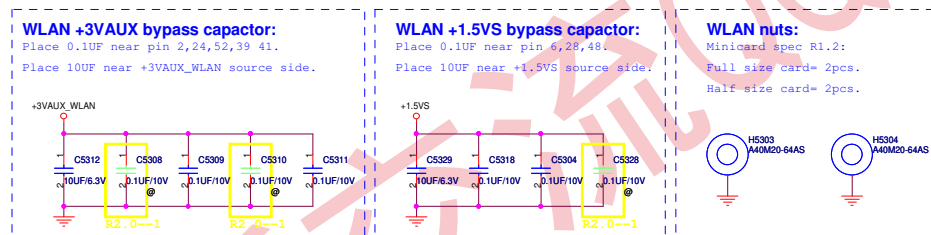


# HDD (2nd)



## USB ports



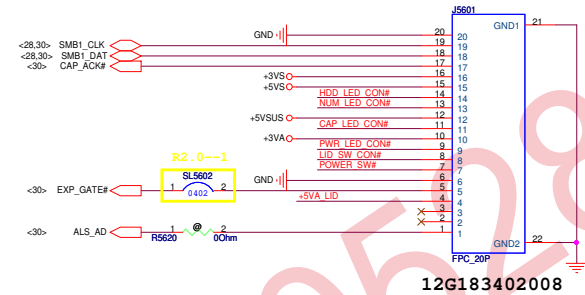
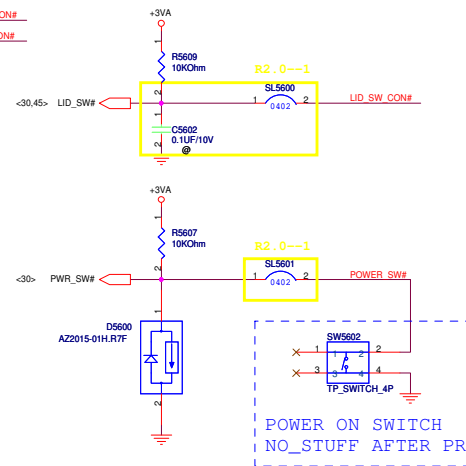
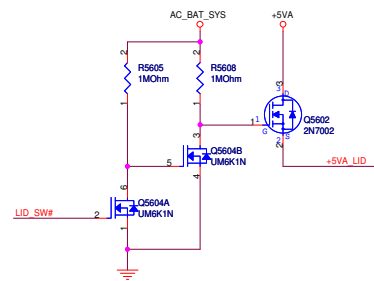


图纸交流QQ : 252670528

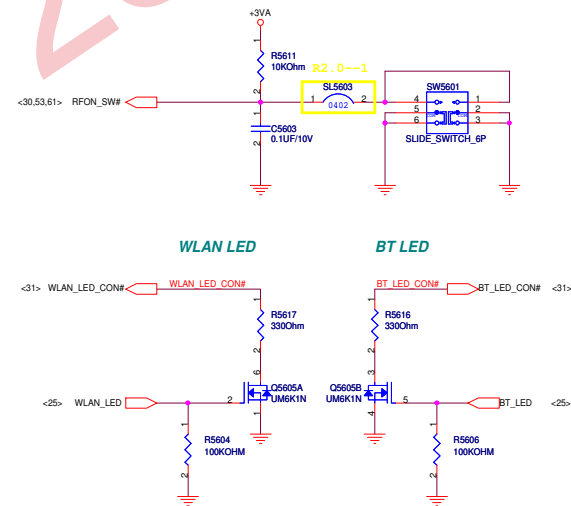
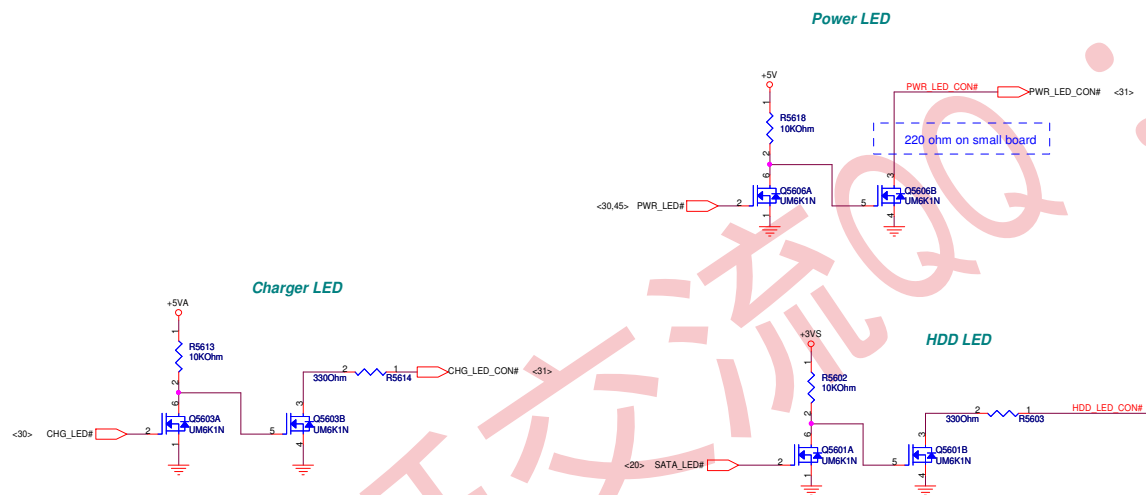
PEGATRON		Title : BAR_****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	54 of 99

图纸交流QQ : 252670528

PEGATRON		Title : SIO ****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
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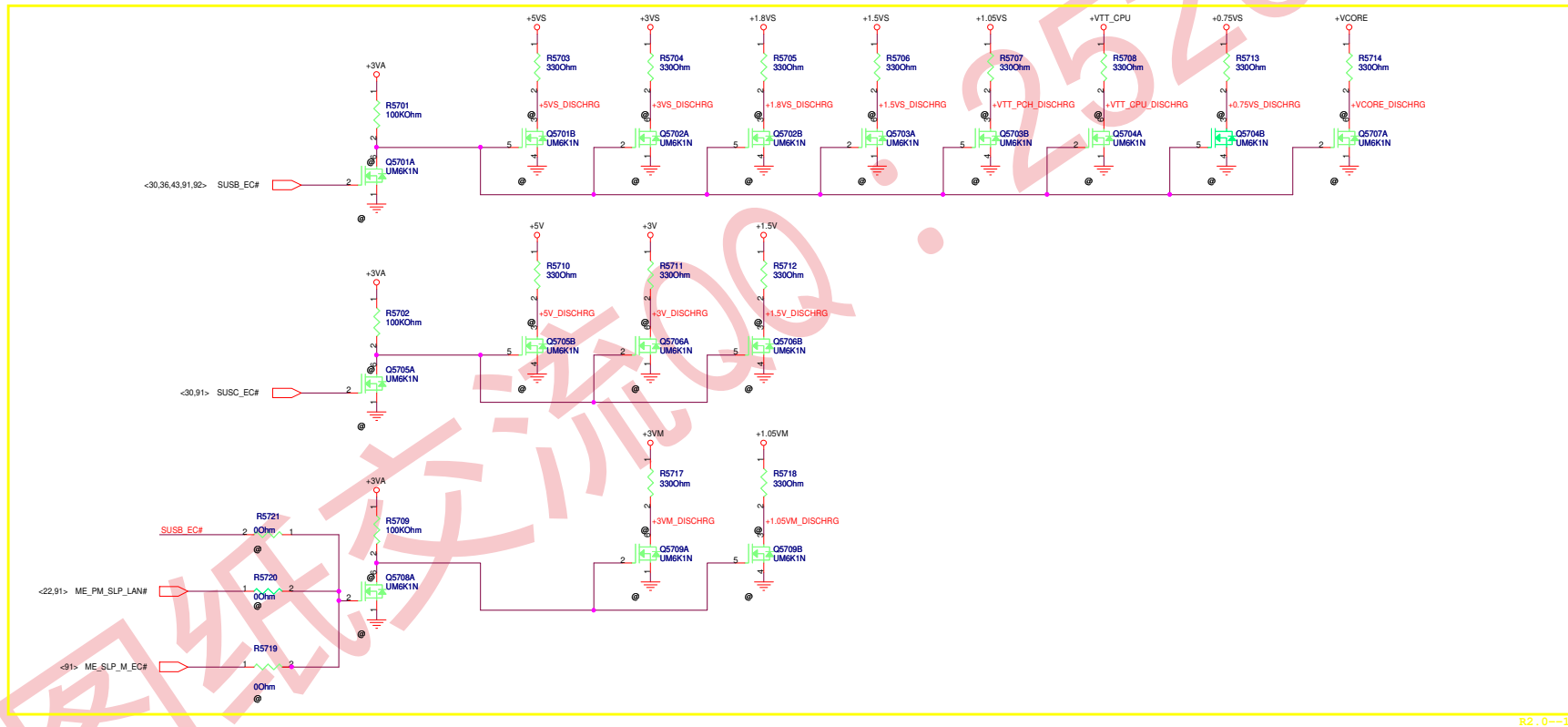
12G183402008



+3V_A	+3V_A	<20,30,57,81,90,93>
+3V_S	+3V_S	<29,48,80,91,92>
+5V_SUS	+5V_SUS	<27,81,91>
+5V_A	+5V_A	<31,81,82,83>
+5V_O	+5V	<31,36,44,45,52,57,65,69,91>
+5V_S	+5V_S	<27,30,31,37,45,46,48,50,51,57,70,80,91>
AC_BAT_SYS	AC_BAT_SYS	<70,80,81,82,83,88>



+3VA +3VA <20,30,56,81,90,93>  
 +VCORE +VCORE <6,69,80>  
 +VGFX\_CORE +VGFX\_CORE  
 +VTT\_CPU +VTT\_CPU <3,6,7,25,26,27,29,32,82>  
 +0.75VS +0.75VS <16,17,83>  
 +1.05VS +1.05VS <26,27,69,91>  
 +1.5VS +1.5VS <26,43,53,64,91>  
 +1.8VS +1.8VS <6,26,38,70,85>  
 +3VS +3VS <29,48,80,91,92>  
 +5VS +5VS <27,30,31,37,45,46,48,50,51,56,70,80,91>  
 +1.5V +1.5V <3,6,16,69,83>  
 +3V +3V <24,33,43,45,61,64,69,91>  
 +5V +5V <31,36,44,45,52,56,65,69,91>  
 +1.05VM\_LAN +1.05VM\_LAN  
 +3VM +3VM <26,28,53,91,92>  
 +1.05VM +1.05VM <27,69,91,92>



R2, 0--1

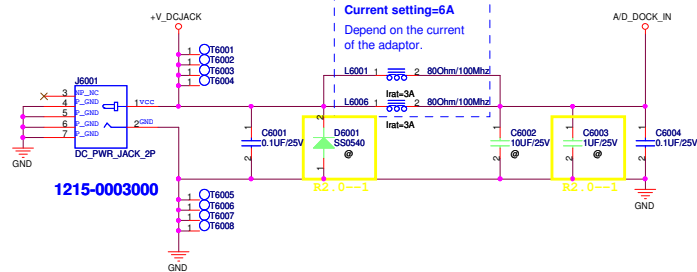
图纸交流QQ : 252670528

PEGATRON		Title : PCI ****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	56 of 99

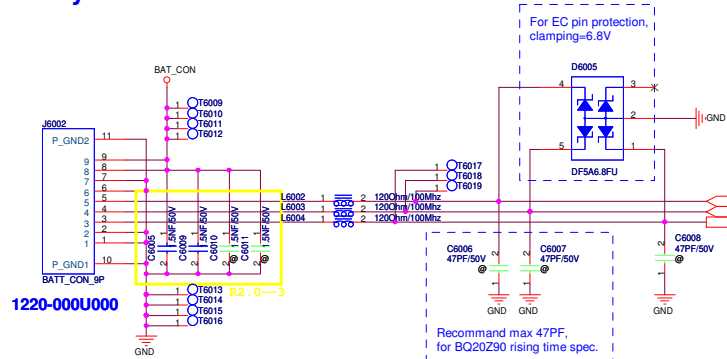
图纸交流QQ : 252670528

PEGATRON		Title : DJ_****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	59 of 99

## DC Jack



## Battery Connector

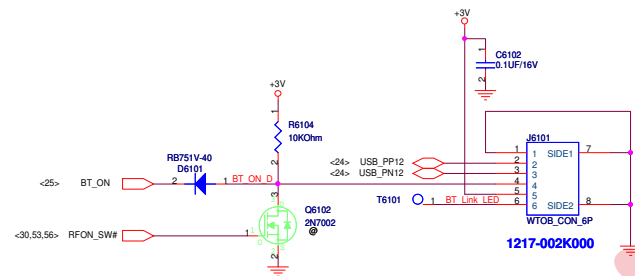


+VCC_RTC	+VCC_RTC	<20,27>
+3VA_EC	+3VA_EC	<30,32>
+3VA	+3VA	<20,30,56,57,81,90,93>
+5VA	+5VA	<31,56,81,82,83>
+3VSUS	+3VSUS	<27,30,33,34,37,53,81,82,92>
+5VSUS	+5VSUS	<27,56,81,91>
+12VSUS	+12VSUS	<28,81,91>
+1.5V	+1.5V	<3,6,16,57,69,83>
+3V	+3V	<24,33,43,45,57,61,64,69,91>
+5V	+5V	<31,36,44,45,52,56,57,65,69,91>
+12V	+12V	<37,91>
+0.75VS	+0.75VS	<16,17,57,83>
+1.05VS	+1.05VS	<26,27,57,69,91>
+1.5VS	+1.5VS	<26,43,53,57,64,91>
+1.8VS	+1.8VS	<6,26,38,57,70,85>
+3VS	+3VS	<29,48,80,91,92>
+5VS	+5VS	<27,30,31,37,45,46,48,50,51,56,57,70,80,91>
+12VS	+12VS	<28,45,91>

AC_BAT_SYS_INV	AC_BAT_SYS_INV	<45,88>
AC_BAT_SYS	AC_BAT_SYS	<56,70,80,81,82,83,88>
AID_DOCK_IN	AID_DOCK_IN	<88>
BAT_CON	BAT_CON	<88>

+1.5V_DDR3	+1.5V_DDR3	<16,17,18>
+VTT_CPU	+VTT_CPU	<3,6,7,25,26,27,29,32,57,82>
+VCORE	+VCORE	<6,57,69,80>
+VGFX_CORE	+VGFX_CORE	
+VTT_PCH_ORG	+VTT_PCH_ORG	<21,22,26,27>
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	<20,26,27>
+1.05VM_ORG	+1.05VM_ORG	<27>
+V_NVRAM_VCCQ	+V_NVRAM_VCCQ	<26>
M_VREFCA_DIMM0	M_VREFCA_DIMM0	<16,18>
M_VREFDQ_DIMM0	M_VREFDQ_DIMM0	<16,18>
M_VREFCA_DIMM1	M_VREFCA_DIMM1	<17,18>
M_VREFDQ_DIMM1	M_VREFDQ_DIMM1	<17,18>

## BLUETOOTH



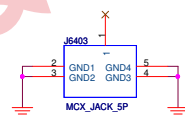
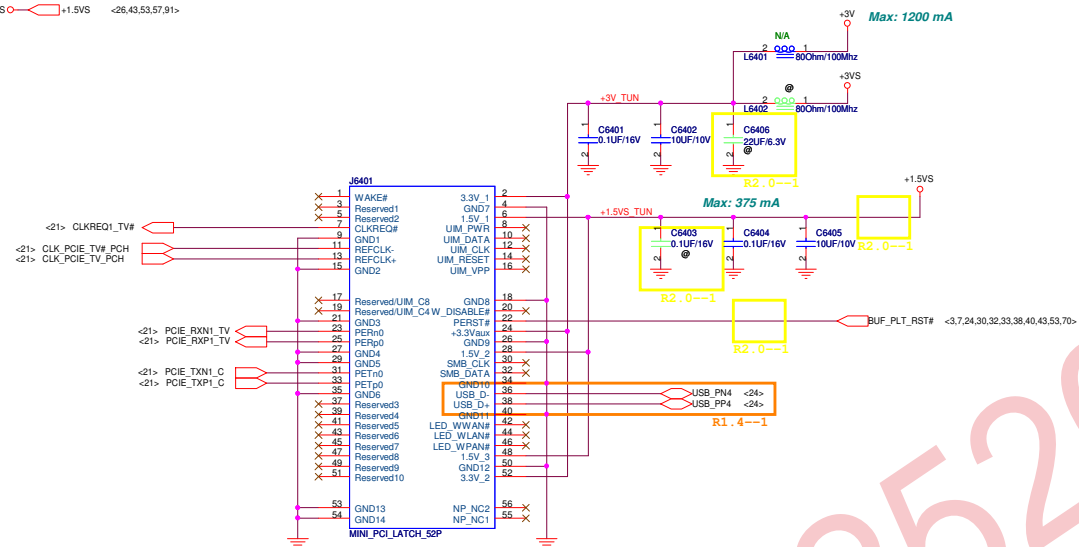
图纸交流QQ : 252670528

PEGATRON		Title : TPM_****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
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图纸交流QQ : 252670528

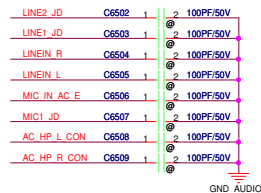
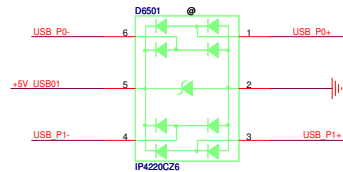
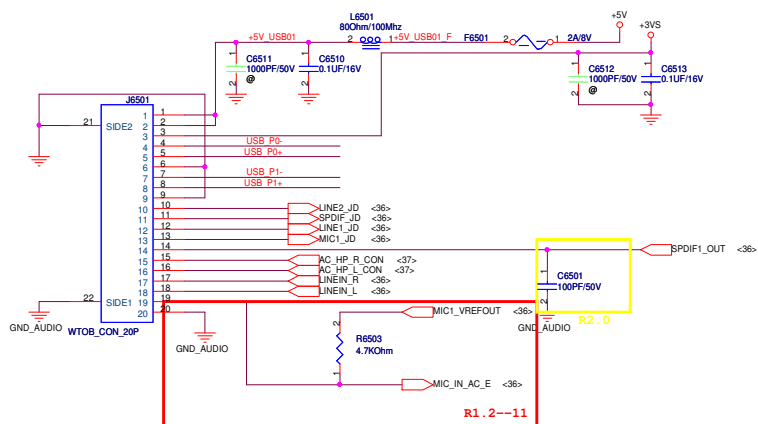
PEGATRON		Title : FP ****	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
Date: Friday, July 31, 2009		Sheet	63 of 99

+3V  +3V <24,33,43,45,57,61,69,91>  
 +3VS  +3VS <29,48,80,91,92>  
 +1.5VS  +1.5VS <26,43,53,57,91>

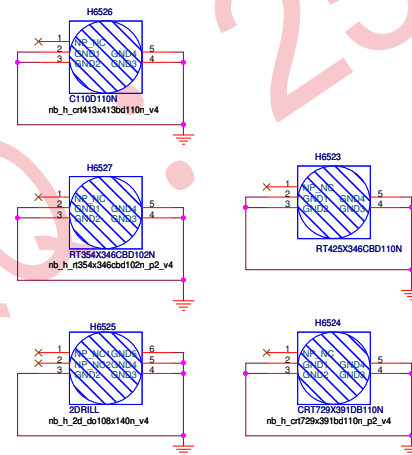
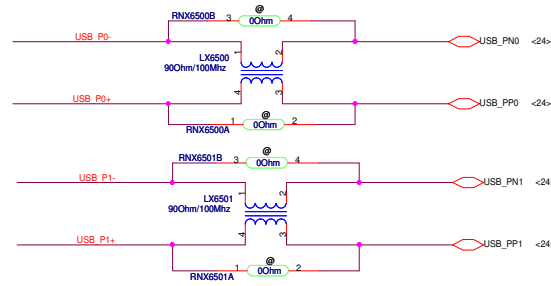


图纸交流QQ: 252670528

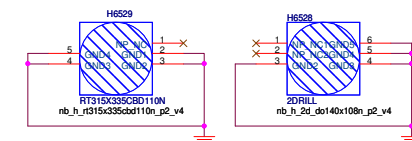




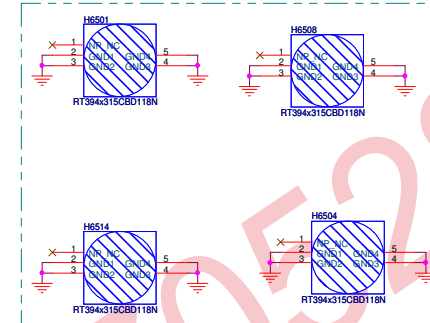
+3VS <29,48,80,91,92>  
+5V <31,36,44,45,52,56,57,69,91>



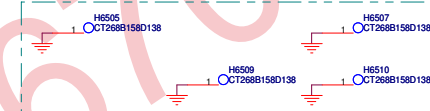
Screw Hole M



Screw Hole A



Screw Hole B



Screw Hole C



Screw Hole F



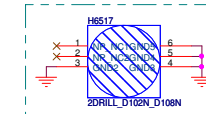
Screw Hole H



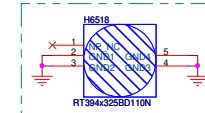
Screw Hole I



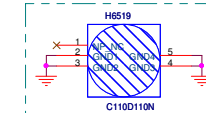
Screw Hole J



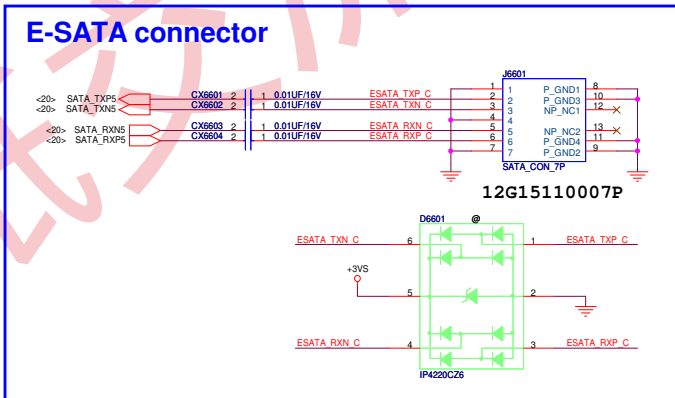
Screw Hole K



Screw Hole L



+3VS ○ □ +3VS <29,48,80,91,92>  
+1.8VS ○ □ +1.8VS <6,26,38,57,70,85>

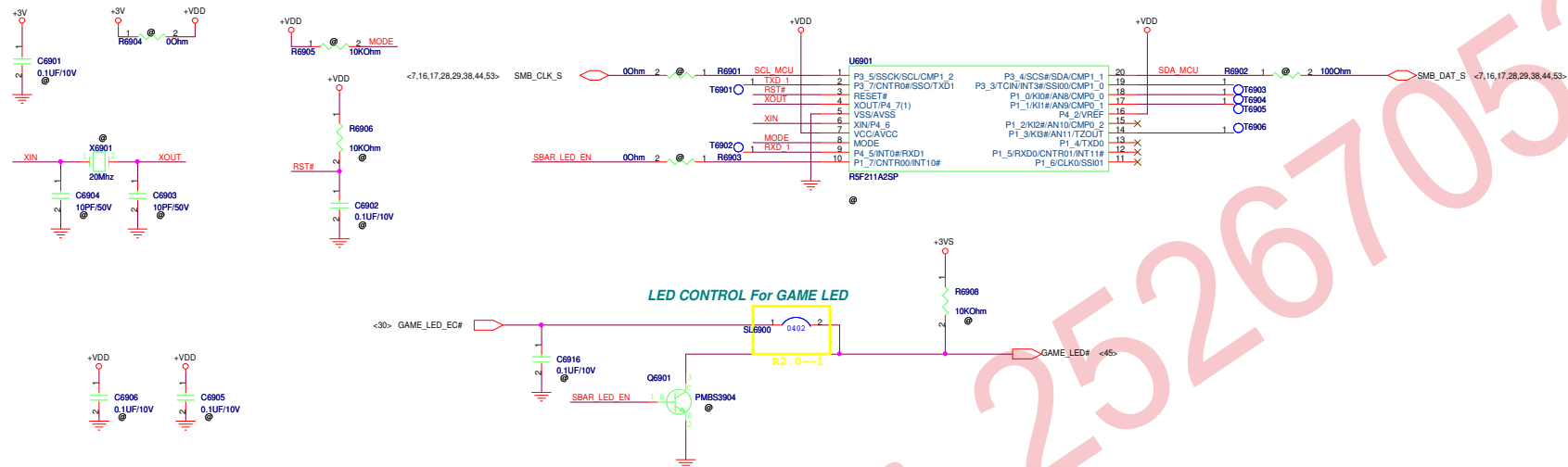




图纸交流QQ : 252670528

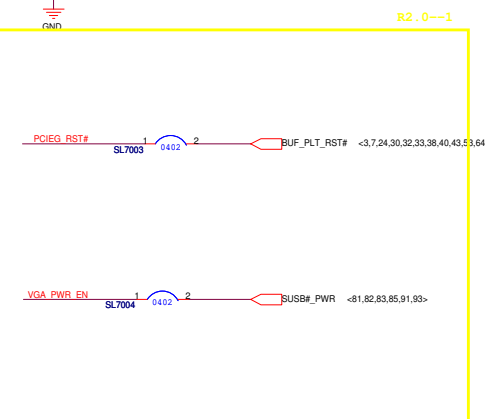
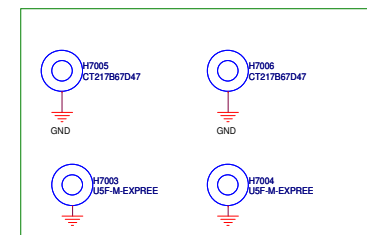
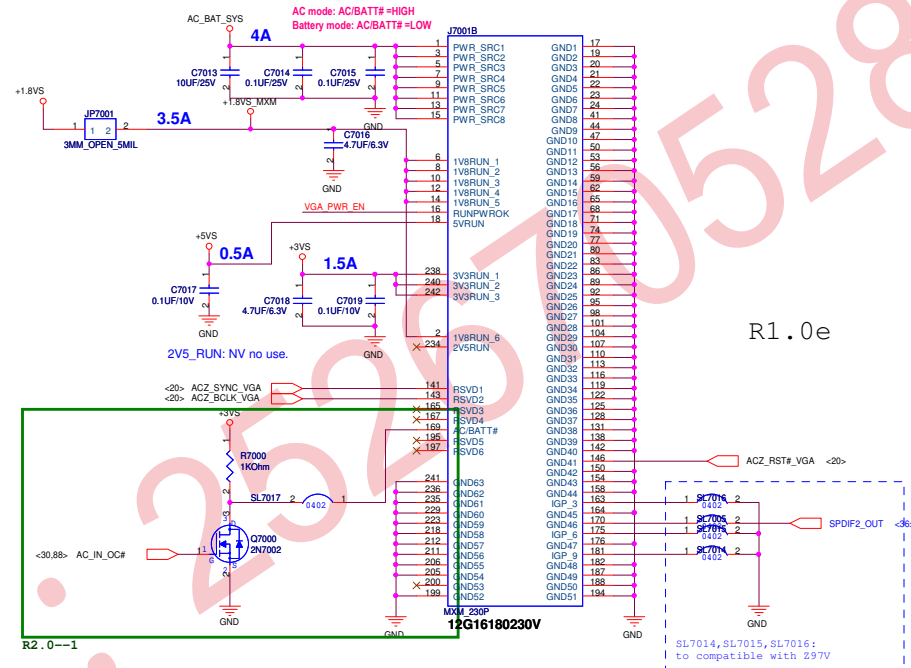
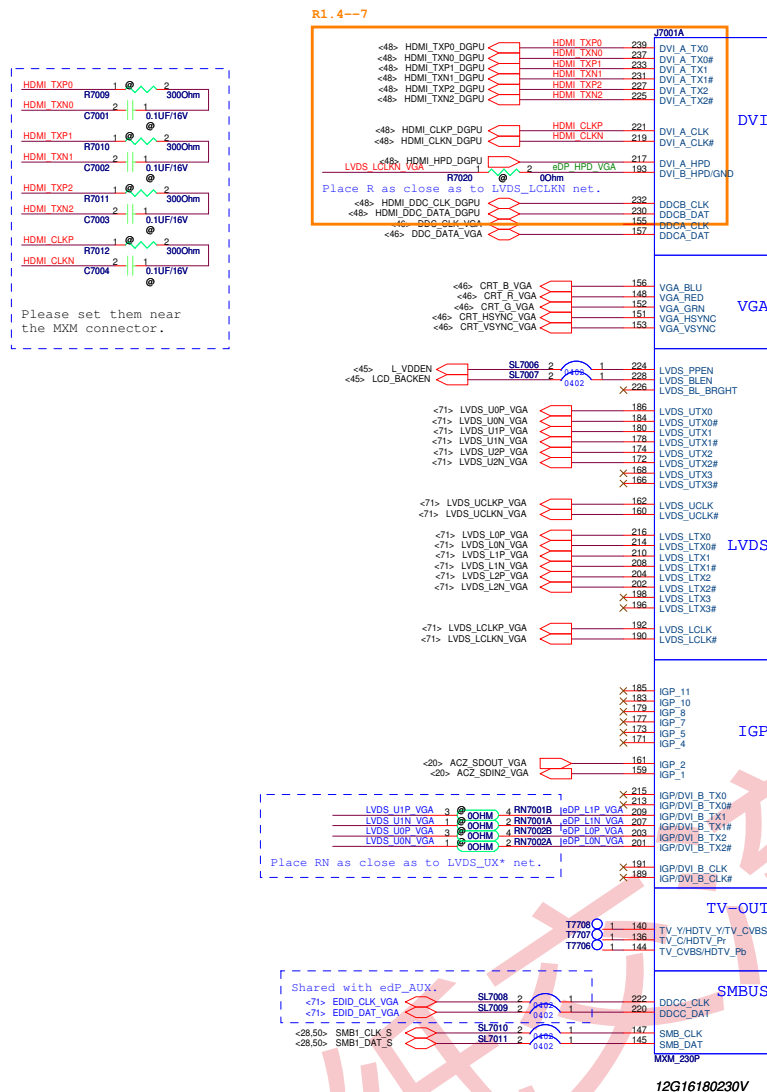
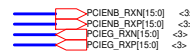
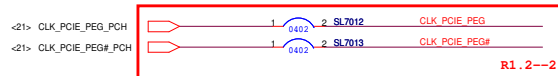
PEGATRON		Title : OTH_LCM	
BU2RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
C	G60J		1.4
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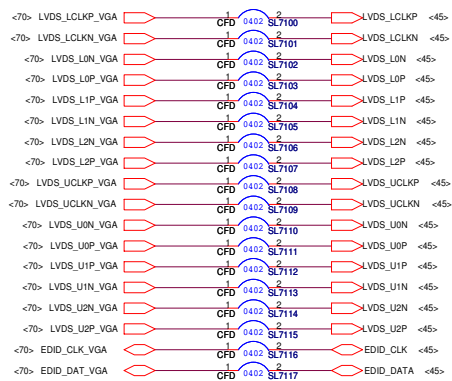
+3V  +3V <24,33,43,45,57,61,64,91>  
+3VS  +3VS <29,48,80,91,92>



The image displays a collection of 24 circuit diagrams, each representing a different electronic configuration. The diagrams are organized into two columns and twelve rows. Each diagram features a component identifier (such as C6907, C6908, C6909, C6910, C6911, C6912, C6913, C6914, C6915, C6917, C6918, C6919, C6920, C6921, C6922, C6923, C6924, C6925, C6926, C6927, C6928, C6929, C6930, C6931, C6932, C6933, C6934, C6935, C6936, C6937) and a resistor value (0.1UF10V). The input and output voltage levels are specified for each circuit, including +5V, +1.05VS, +1.5V, +3VS, +1.05VM, and +VCORE. The diagrams illustrate various signal conditioning and voltage regulation techniques. A large, diagonal red watermark reading 'www.electronicshub.org' is present across the entire image.

<b>PEGATRON</b>		Title : <b>OTH_GAME-LED</b>	
<b>BU2/RD1</b>		Engineer: <b>Kenny Wu</b>	
Size <b>C</b>	Project Name <b>G60J</b>		Rev <b>1.4</b>
Date: <b>Friday, July 31, 2009</b>		Sheet	<b>69</b> of <b>99</b>





+5VS <27,30,31,37,45,46,48,50,51,56,57,70,80,91> +5VS

图纸交流QQ: 252670528

图纸交流QQ : 252670528

PEGATRON		Title : VGA(3) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
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图纸交流QQ : 252670528

PEGATRON		Title : VGA(4) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
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图纸交流QQ : 252670528

PEGATRON		Title : VGA(5) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet	74	of 99

图纸交流QQ : 252670528

PEGATRON		Title : VGA(6) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet 75 of 99		1

图纸交流QQ : 252670528

PEGATRON		Title : VGA(7) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet 76 of 99		1

图纸交流QQ : 252670528

PEGATRON		Title : VGA(8) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet	77	of 99

图纸交流QQ : 252670528

PEGATRON		Title : VGA(9) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet 78 of 99		1

图纸交流QQ : 252670528

PEGATRON		Title : VGA(10) ****	
BU2/RD1		Engineer: Kenny Wu	
Size	Project Name		Rev
Custom	G60J		1.4
Date: Friday, July 31, 2009	Sheet 79 of 99		

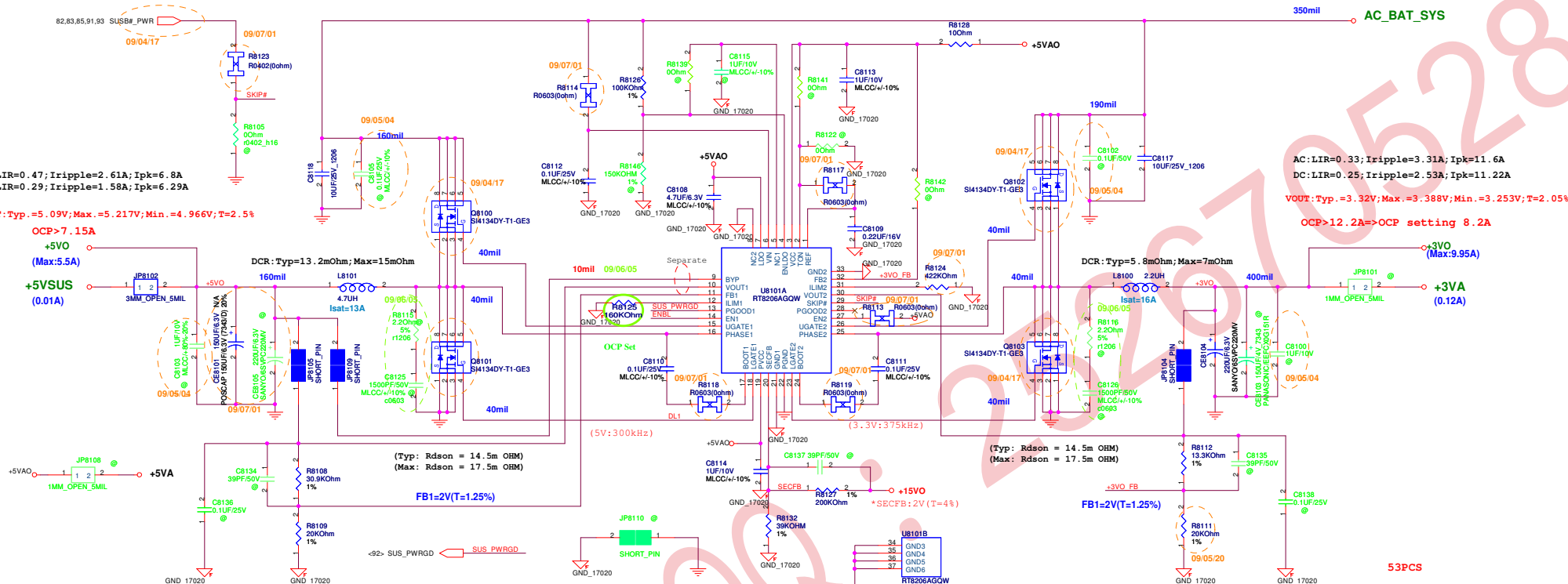




SKIP:  
GND : DEM operation;  
REF : Ultrasonic Mode operation;  
VCC : PWM operation.

TON: (5V/3.3V)  
VCC: (200kHz/250kHz)  
REF: (300kHz/375kHz)  
GND: (400kHz/500kHz)

VENLDO:  
Rising Edge:Max:2V;Typ:1.6V;Min:1.2V  
Falling Edge:Max:1.06V;Typ:1V;Min:0.94V

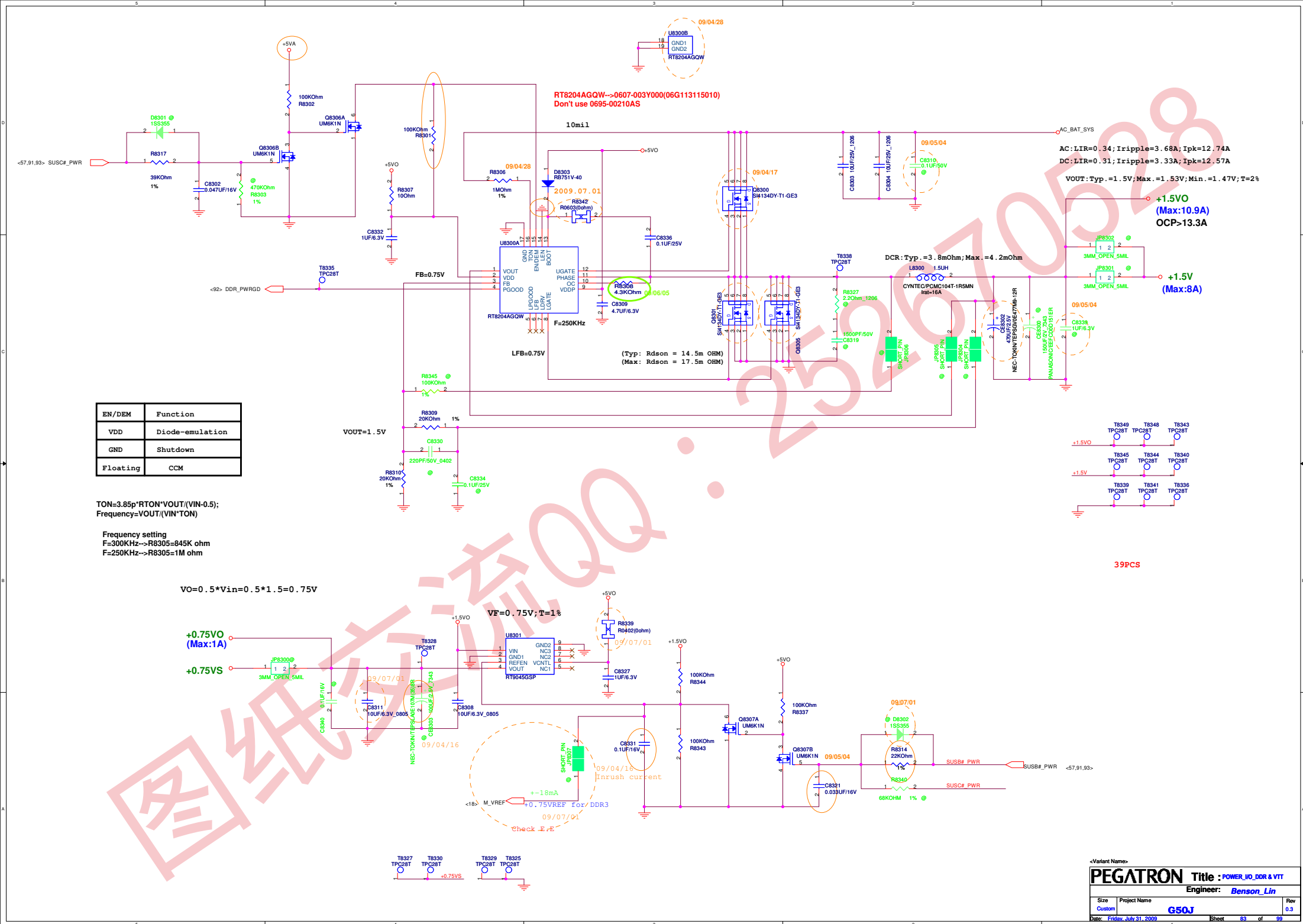


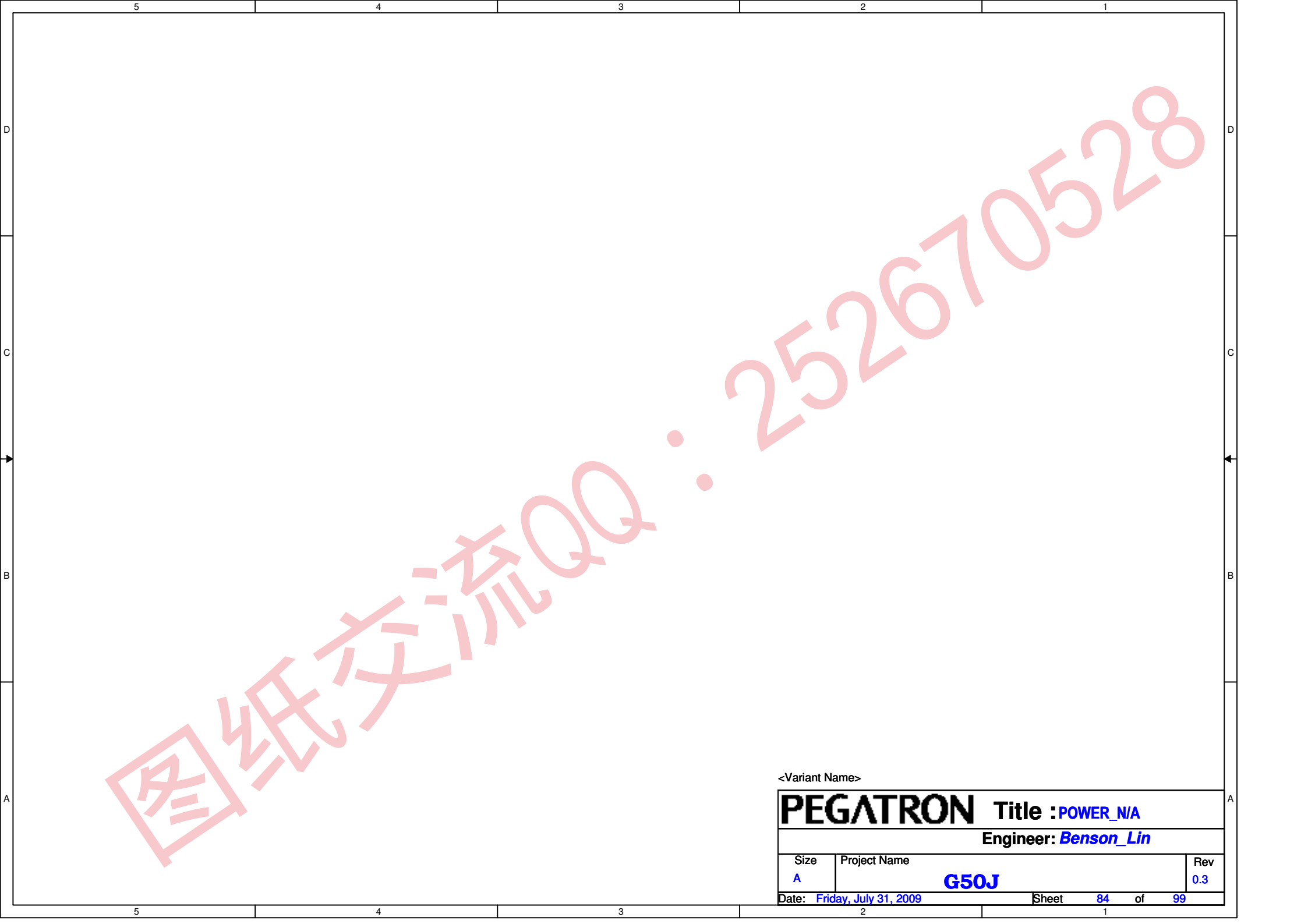
TOTAL COUNT : 38 PCS

<Variant Name>

PEGATRON Title :POWER_SYSTEM			
Engineer: Benson_Lin			
Size	Project Name		Rev
Custom	G50J		0.1
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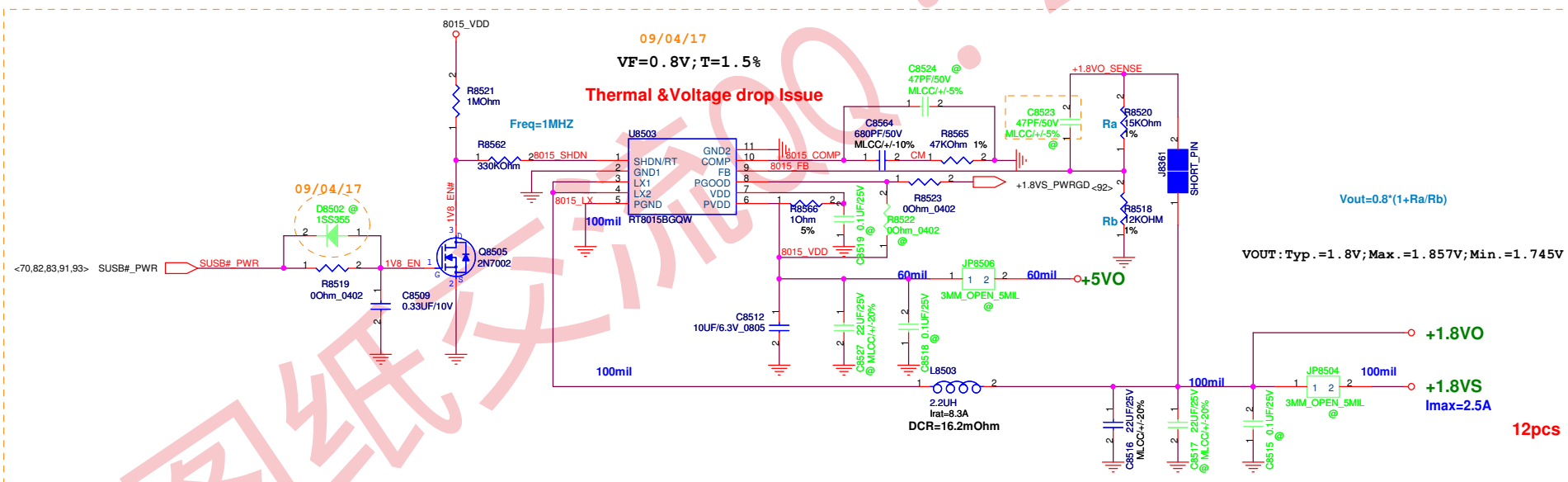




<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
Engineer: <b>Benson_Lin</b>			
Size <b>A</b>	Project Name <b>G50J</b>		Rev <b>0.3</b>
Date: <b>Friday, July 31, 2009</b>		Sheet <b>84</b> of <b>99</b>	

@---R1.3(ASUS P.M Change K/P,E.E Change power budget)



RT8015B=>R8523mount;R8522unmount;  
RT8015A=>R8522mount;R8523unmount

<Variant Name>

**PEGATRON** Title : **POWER +1.8VS**

Engineer: **Benson\_Lin**

Size	Project Name	Rev
Custom	<b>G50J</b>	0.3
Date: Friday, July 31, 2009	Sheet 85 of 99	

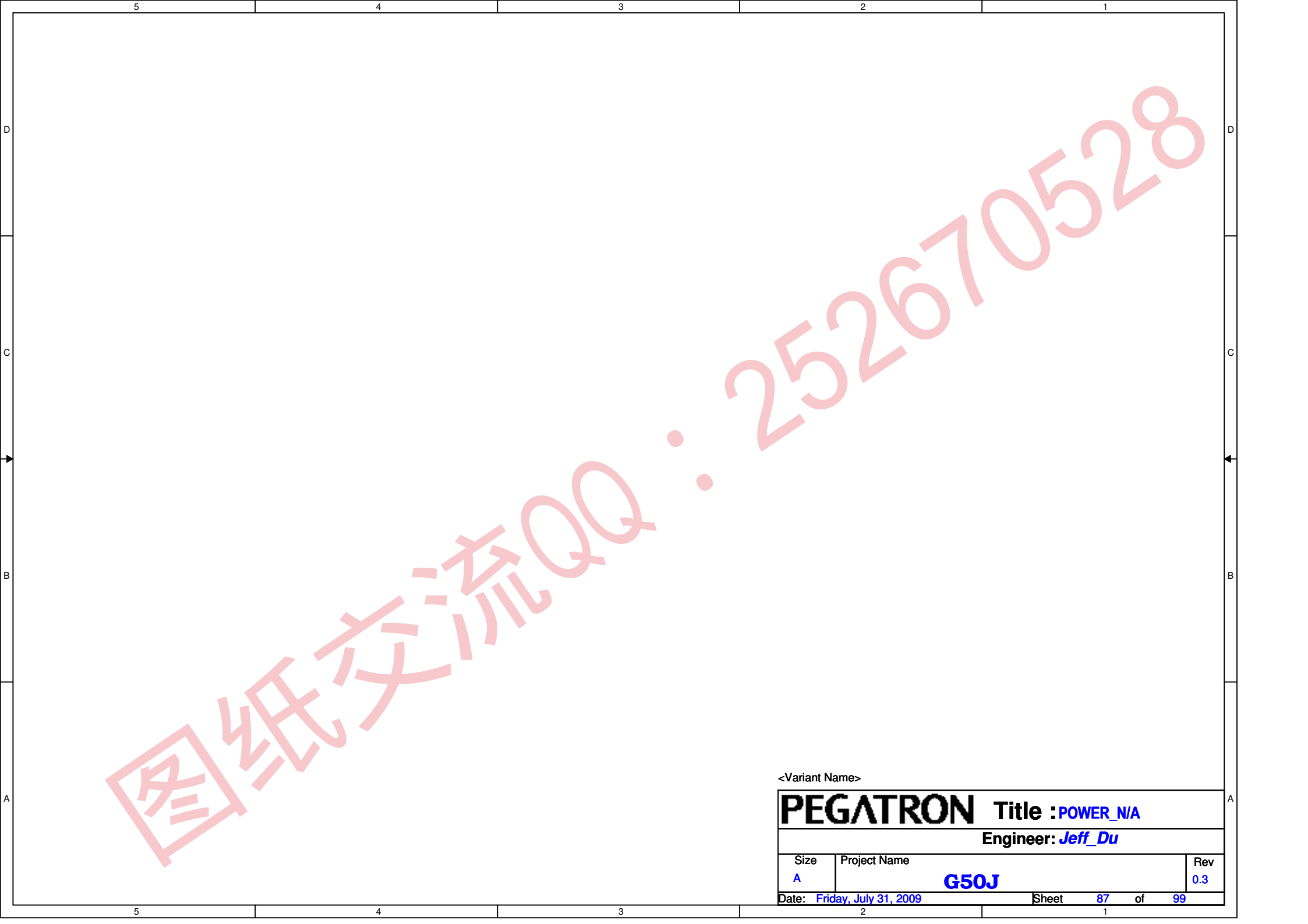
图纸交流QQ: 252670528

44pcs

G60J CPU use Clarkfiel,so don't need VGA power

<Variant Name>

PEGATRON		Title :POWER_VGFX_CORE	
		Engineer: Benson Lin	
Size	Project Name	Rev	
Custom	G50J	0.3	
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<Variant Name>

<b>PEGATRON</b>			Title : <b>POWER_N/A</b>		
Engineer: <b>Jeff_Du</b>					
Size <b>A</b>	Project Name <b>G50J</b>				Rev <b>0.3</b>
Date: <b>Friday, July 31, 2009</b>			Sheet	<b>87</b>	of <b>99</b>

Adaptor =120W, 19V/6.32A

16.857V < ACIN <18.014V

120W/90W:R8801=15m OHM(11G21DR0151110)

65W:R8801=20m OHM(10G21DR02015110)

09/07/01(change 1206 size for cost down)

09/07/03(for EMI)

AC\_BAT\_SYS

BAT\_CON

AC\_BAT\_SYS\_INV

AC\_BAT\_SYS\_INV to Inverter connect,  
Power trace =60mil(min), Put JP8804 close to Q8800

12.641V(min) < VBAT-12.515(Typ) < 12.768V(Max)

BAT  
2P/3P, 2400mAh

MAX17015 VBAT setting:

VCTL connect to GND,VFB=2.1V

VBAT=2.1\*(R8819+R8828)/R8828

Fix R8828 to 10K, adjust R8819

R8819=30K,VBAT=8.4V(2cell)

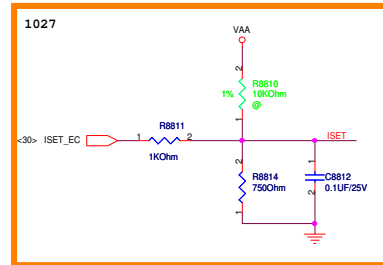
R8819=49.9K,VBAT=12.579V(3cell)

R8819=69.8K,VBAT=16.758V(4cell)

VCTL connect to GND,VFB=2.1V

VBAT=2.1\*(R8819+R8828)/R8828

12.641V(min) < VBAT-12.515(Typ) < 12.768V(Max)



ISET_EC	ISET(Voltage)	CHG_CURRENT	
0.1294V	0.055V	0.157A	PRECHG
2.0188V	0.865V	2.472A(0.52C)	Quick CHG

$I_{chg} = (240m / R_{S2}) * (V_{ISET} / V_{AA})$

$I_{chg} = (240m / 20m) * (0.055 / 4.2) = 0.157A$

$I_{chg} = (240m / 20m) * (0.865 / 4.2) = 2.4714A$

VSET_EC	BAT	
1.4106V	12.545V	ON
3.2871V	5.519V	OFF

<Variant Name>

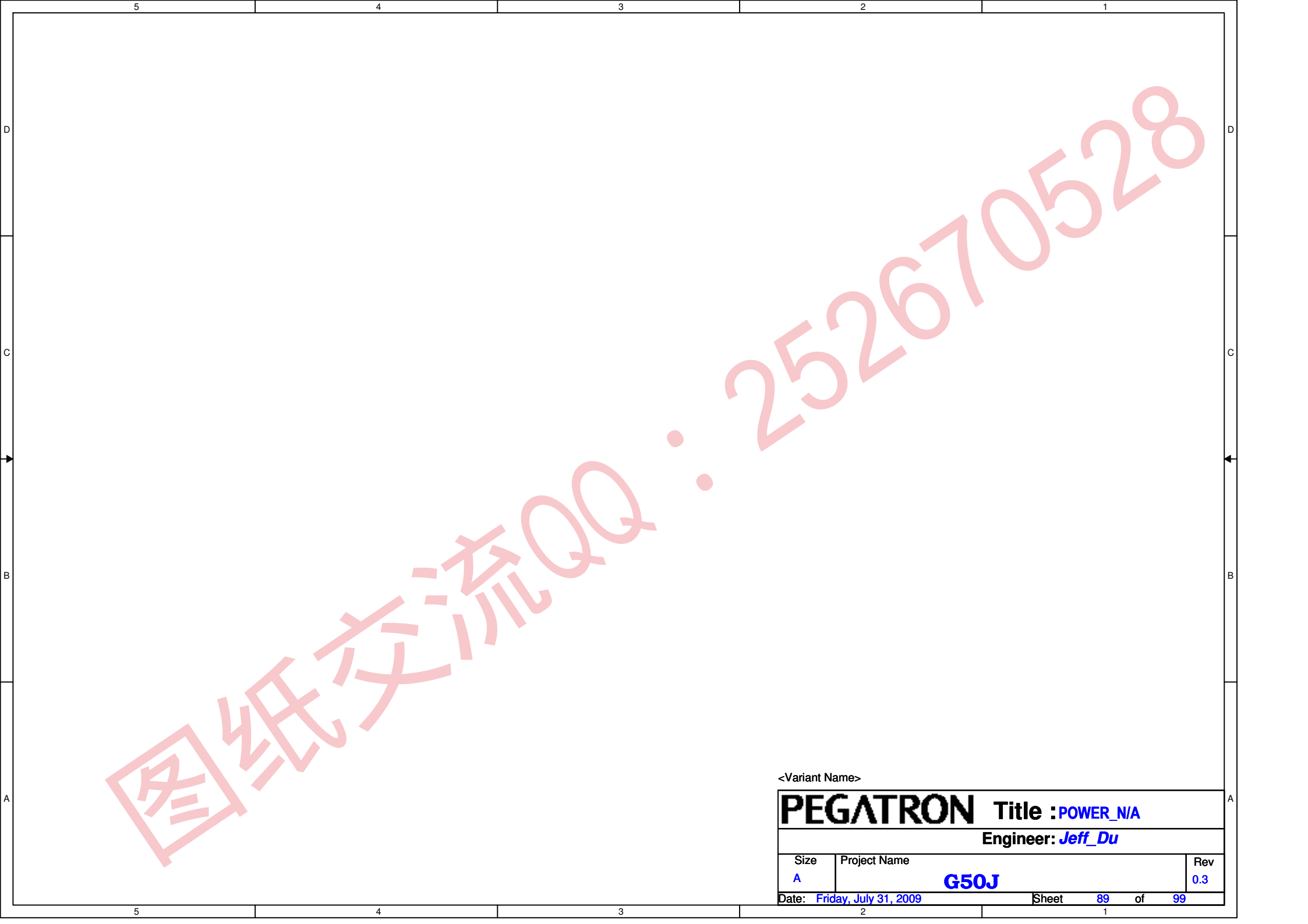
**PEGATRON** Title :CHARGER\_201

Engineer: Benson\_Lin

Size	Project Name	Rev
C	G50J	0.3

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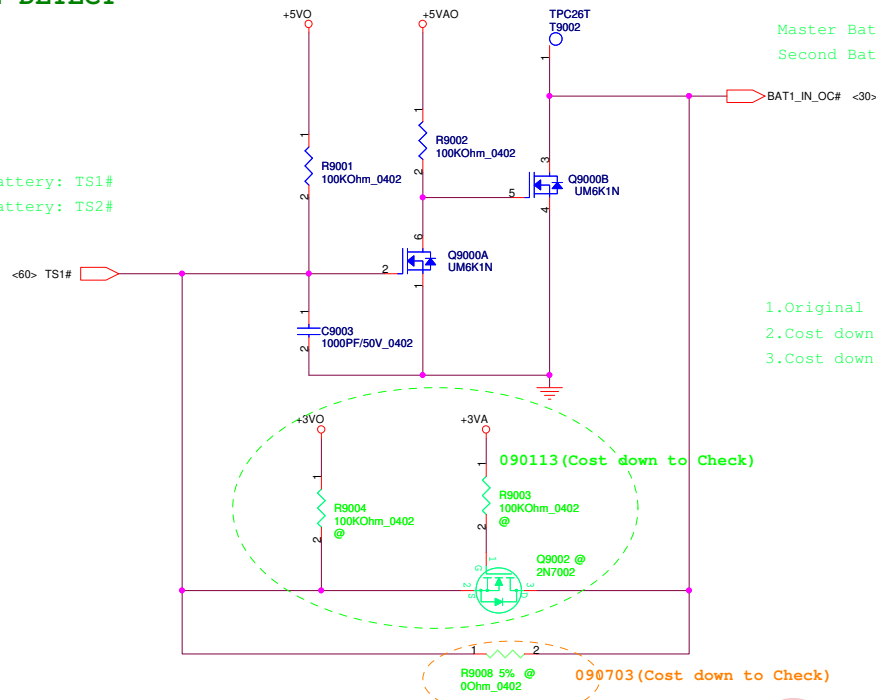


<Variant Name>

<b>PEGATRON</b>			Title : <b>POWER_N/A</b>		
Engineer: <b>Jeff_Du</b>					
Size <b>A</b>	Project Name <b>G50J</b>				Rev <b>0.3</b>
Date: <b>Friday, July 31, 2009</b>			Sheet	<b>89</b>	of <b>99</b>

BATTERY IN DETECT

Master Battery: TS1#  
Second Battery: TS2#



Master Battery: BAT1\_IN\_OC#  
Second Battery: BAT2\_IN\_OC#

ADAPTER IN DETECT

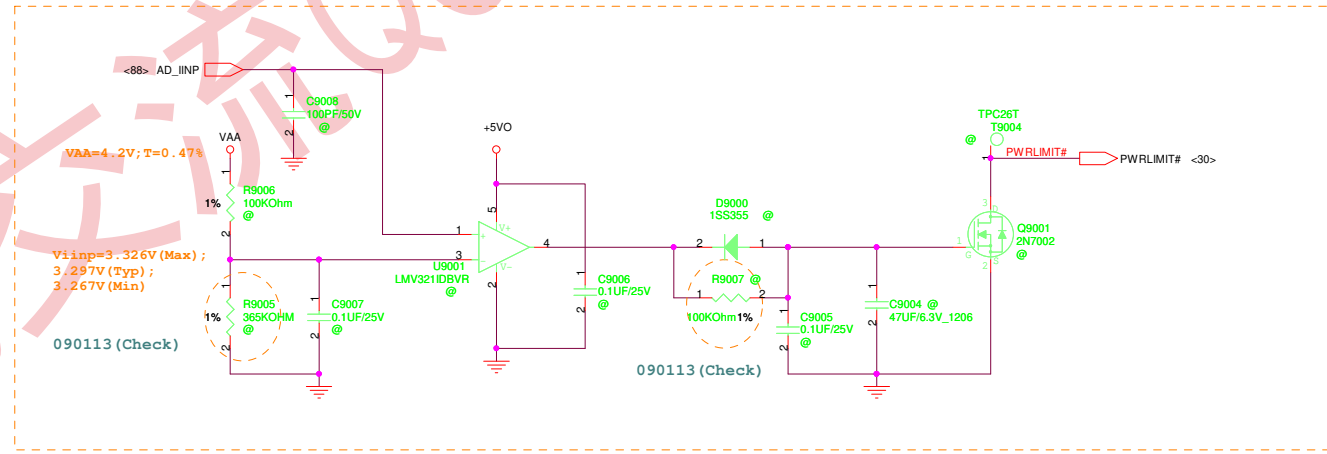
Use MAX17015 IC function to Cost down component

- 1.Original : mount R9001.R9002.C9003.Q9000A.Q9000B
- 2.Cost down : mount R9004.R9003.Q9002.C9003
- 3.Cost down : mount R9008.C9003

POWER LIMIT CIRCUIT

@---09.07.01 (Cost Down)

+2.5Vref delete



Pinput=111.8625W---->Iinput=5.8875A  
RS1=20mohm, Giinp=2.8uA/mV, Riinp=10K  
Iinput=Viinp/(RS1\*Giinp\*Riinp)=Viinp/(20m\*2.8uA/mV\*10K)=5.8875A---->Viinp=3.297V

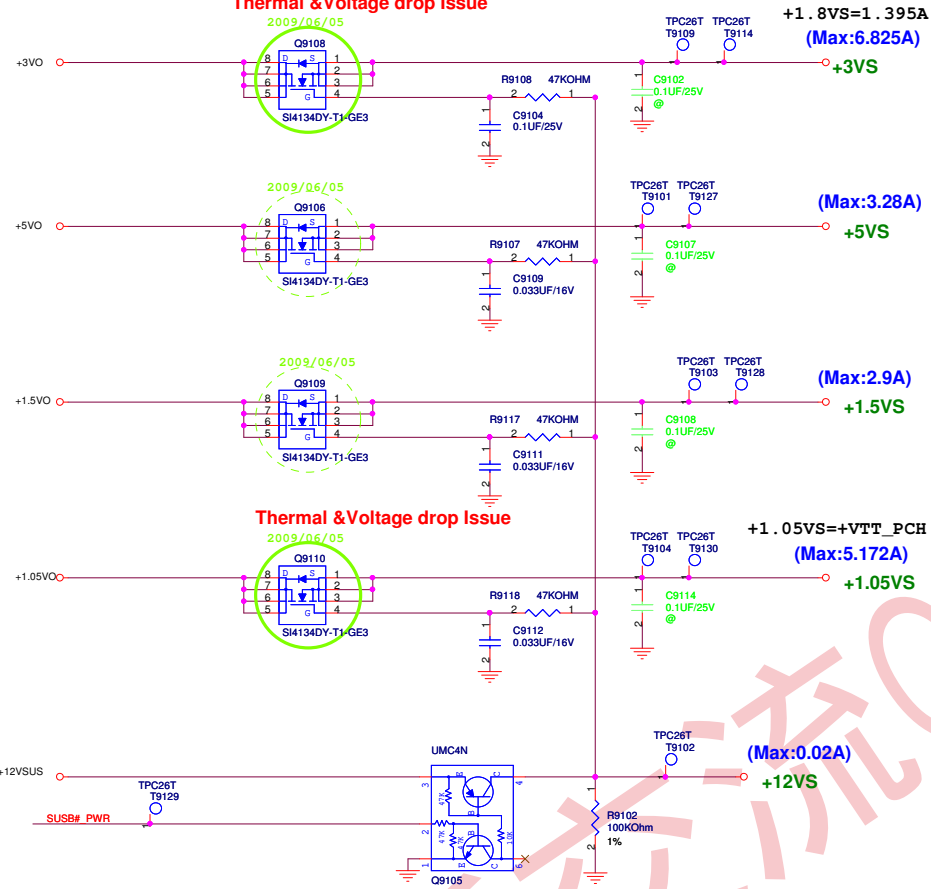
4pcs

<Variant Name>		
PEGATRON Title :POWER_DETECT		
Engineer: Benson_Lin		
Size	Project Name	Rev
Custom	G50J	0.3
Date: Friday, July 31, 2009	Sheet 90 of 99	

# SUSB#\_PWR POWER

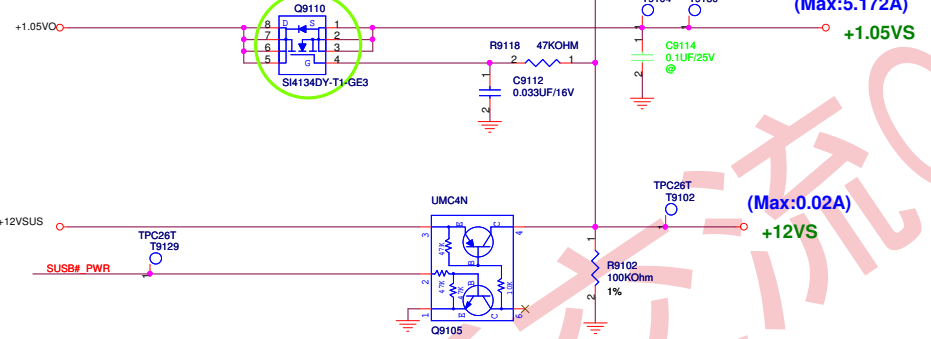
## Thermal & Voltage drop Issue

2009/06/05

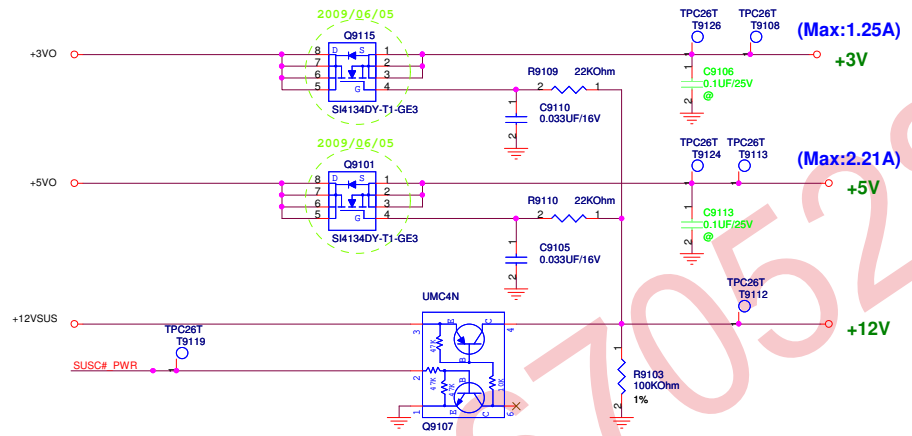


## Thermal & Voltage drop Issue

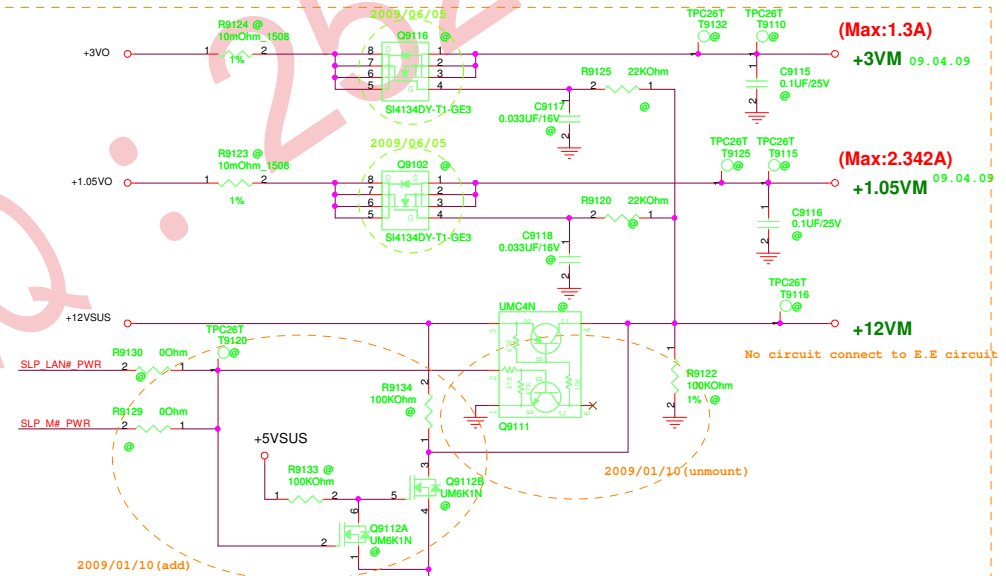
2009/06/05



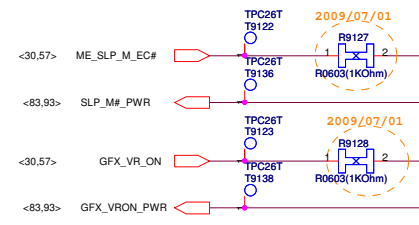
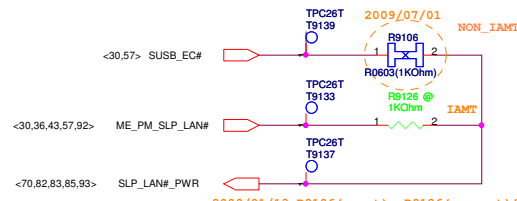
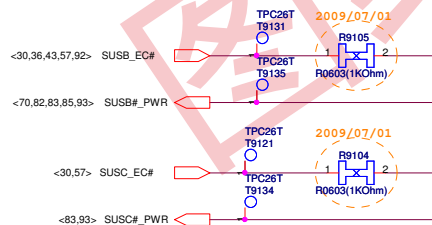
# SUSC#\_PWR POWER



## IAMT POWER @Cost down---PR Unmount (combine with SUSB#\_PWR)



2009/07/01 For power +3VA test; If short +3VA JP point to check power; should be cut off this temp line.



54pcs

<Variant Name>

PEGATRON Title :POWER\_LOAD SWITCH

Engineer: Benson\_Lin

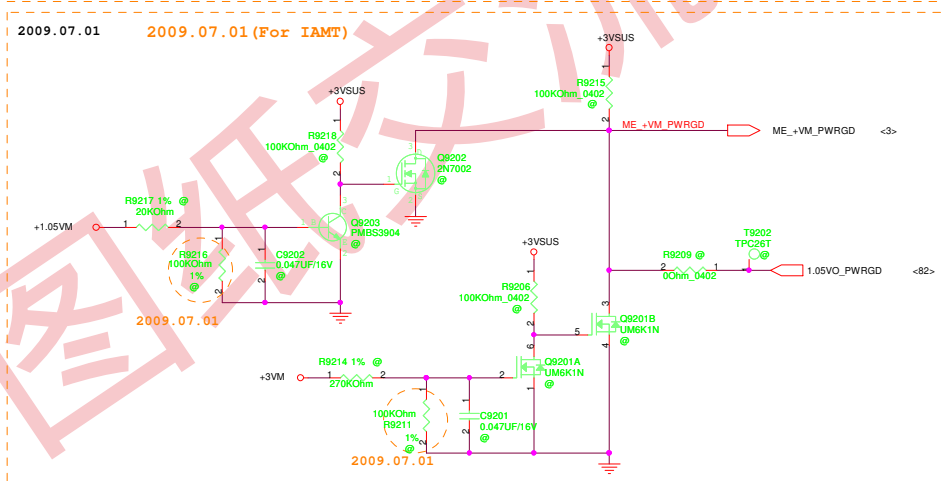
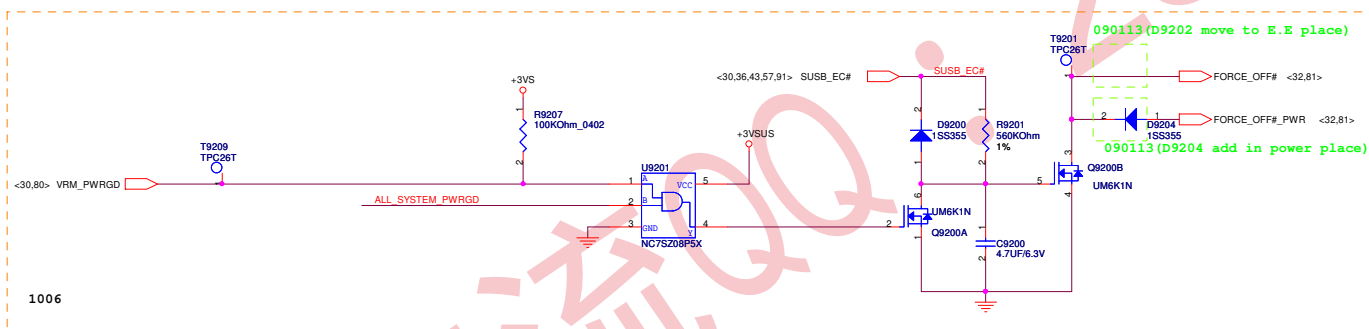
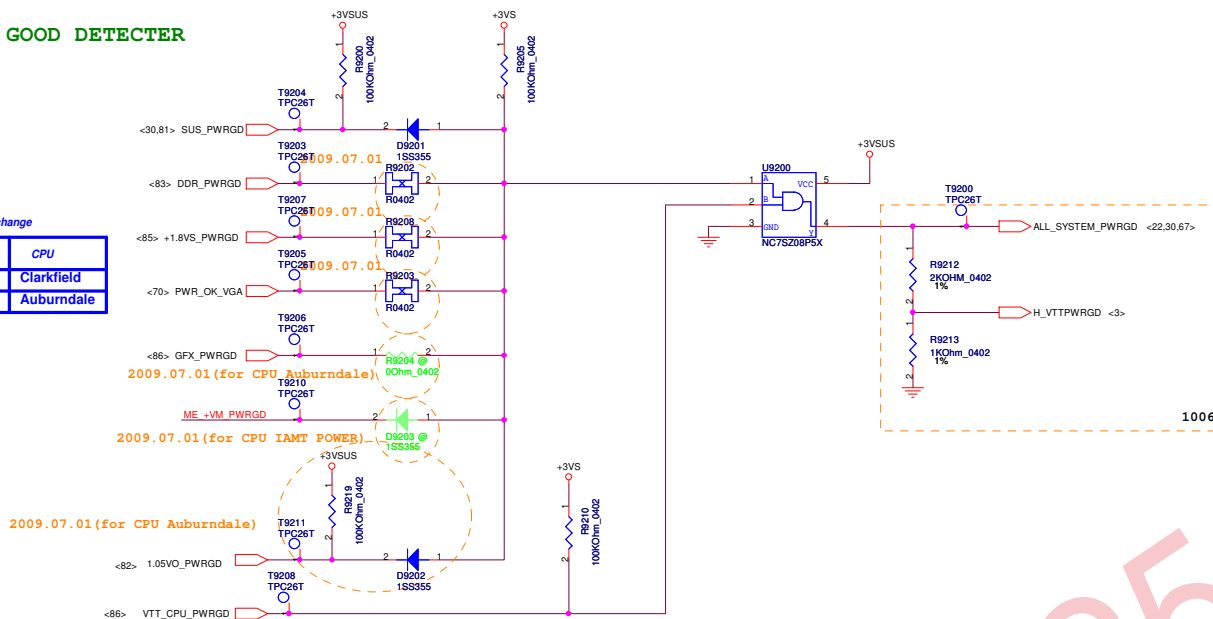
Size: Custom Project Name: G50J Rev: 0.3

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# POWER GOOD DETECTOR

## BOM change

YES/NO	CPU
X	Clarkfield
R9204	Auburndale



AC\_BAT\_SYS <70,80,81,82,83,86,88>  
BAT <88>  
BAT\_CON <60,88>

+3VA <20,30,56,57,81>  
+5VAO <81,85,90>  
+5VA <31,56,81>

+5VO <81,82,83,90,91>  
+3VO <81,91>  
+1.8VO <81,91>  
+0.9VO <81,91>  
+1.05VO <80,82>  
+1.5VO <83,91>

+5VSUS <27,56,81,86>  
+3VSUS <3,21,22,24,25,27,30,33,37,53,70,81,82,92>  
+12VSUS <28,70,81,91>

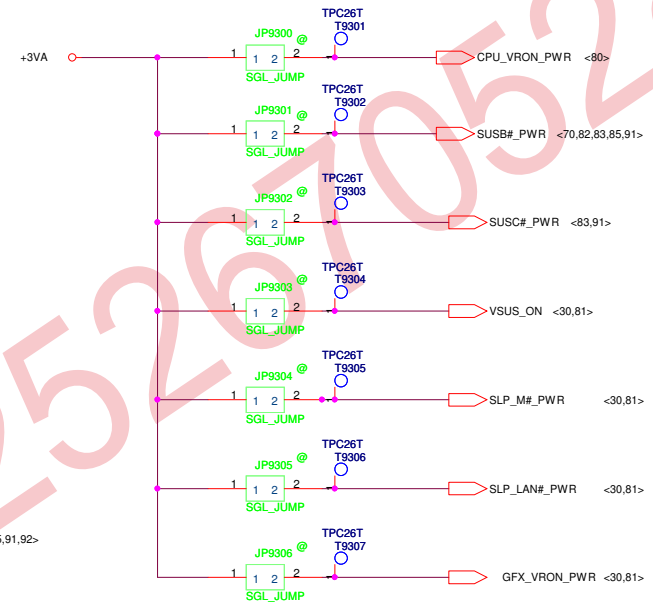
+5V <31,36,44,45,46,52,56,57,65,68,70,85,91>  
+3V <24,31,43,45,57,61,64,68,69,91>  
+12V <37,42,68,91>  
+1.8V <81,91>  
+0.9V <81,91>

+3VS <16,17,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,36,37,40,41,42,43,44,45,46,47,48,50,51,53,56,57,64,65,66,67,70,80,85,91,92>  
+5VS <27,31,37,45,46,47,48,50,51,56,57,71,80,91>  
+12VS <28,45,70,91>

+1.5VS <26,43,53,57,64,70,91>

+VCCP <6,57,80>  
+VCORE <6,57,80>

## FOR POWER TEST



<Variant Name>

**PEGATRON** Title : **POWER SIGNAL**  
Engineer: **Benson\_Lin**

Size	Project Name	Rev
Custom	G50J	0.3
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JUMP must be shorted:

JP1601,JP1801,JP1802,JP2601,JP2602,JP2603,  
JP2701,JP2702,JP2703,JP2704,JP8100,JP8101,  
JP8102,JP8106,JP8205,JP8301,JP8504.

OPTIONAL selection:

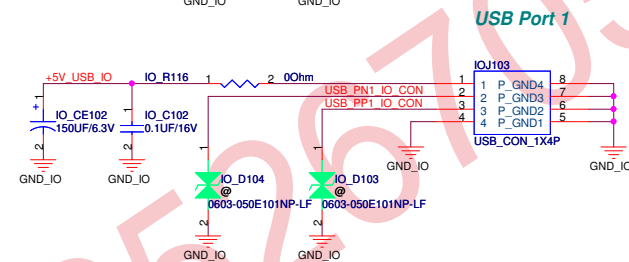
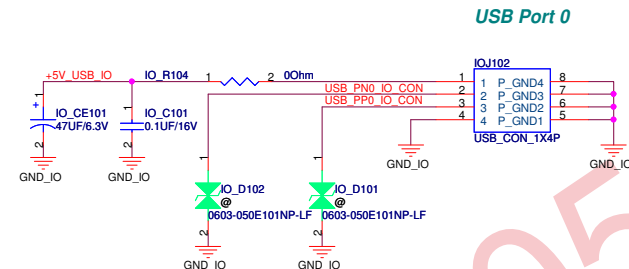
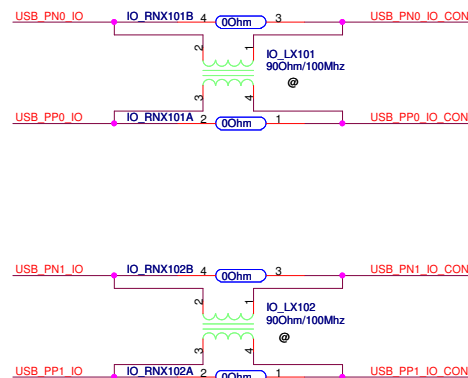
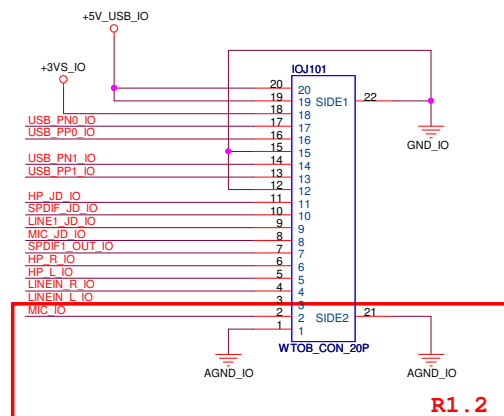
@ -> no-stuff for all  
CFD -> stuff for Clarkfield with MXM  
CFD@ -> no-stuff for Clarkfield with MXM  
AUB -> stuff for Auburndale with MXM (switchable GFX)  
AUB@ -> no-stuff for Auburndale with MXM (switchable GFX)  
IAMT -> stuff for IAMT sku  
IAMT@ -> no-stuff for IAMT sku  
NON\_IAMT -> stuff for non-IAMT sku  
NON\_IAMT@ -> no stuff for non-IAMT sku  
CPU\_XDP -> stuff for CPU XDP using  
CPU\_XDP@ -> no-stuff for CPU XDP using  
PCH\_XDP -> stuff for PCH XDP using  
PCH\_XDP@ -> no-stuff for PCH XDP using

R1.1--> R1.2 Changed List:

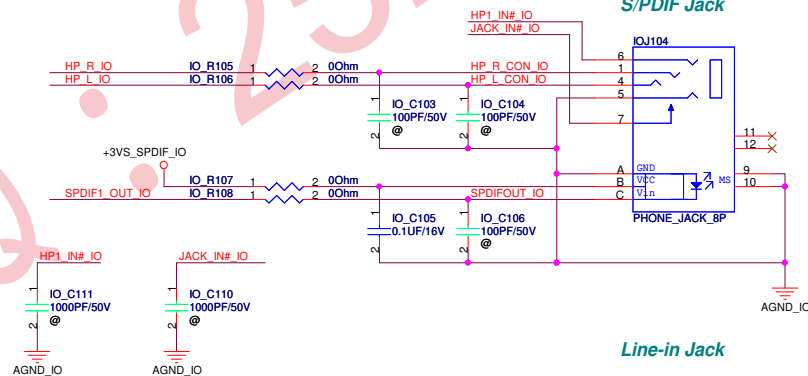
- 1.Refer to #413686.
- 2.For the buffered mode is stable.
- 3.For Deleting PCH XDP, modify P20,P67.
- 4.For MXM 2.1a, modify P21, P70.
- 5.For PCIE CB,modify P40, P24.
- 6.Refer to DG R1.0.
- 7.Del the tested 0ohm.
- 8.For LVDS display on AUB.
- 9.Change DP port from B to D by Intel recommendation.
- 10.For reassigning USB Port, modify P24.
- 11.Repair R1.1 bug.
- 12.For Lighting Keyboard.
- 13.For Non-IAMT.
- 14.Remove PCIE<-->SATA Circuit(P66) for PCH SATA stable.
- 15.For Project SPEC, Del P68.
- 16.Add Second Source.

R1.3--> R1.4 Changed List:

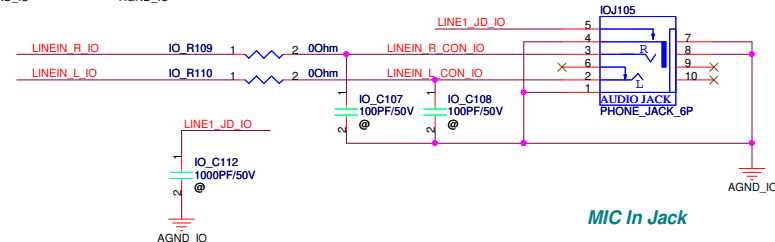
- 1.Intel recommended.
- 2.For G60J SPEC.
- 3.Change CK505 from ICS3362 to ICS3197.
- 4.For PCH GPIO Definition.
- 5.R1.3 bug fixed.
- 6.GLAN from RTL8111C to AR8131
- 7.Add HDMI Switch(PI3HDMI201).
- 8.NV recommended.



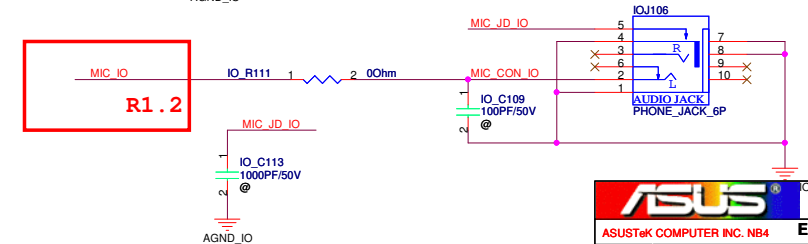
## Headphone &amp; S/PDIF Jack



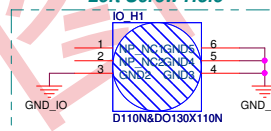
## Line-in Jack



## MIC In Jack



## Left Screw Hole



## Right Screw Hole

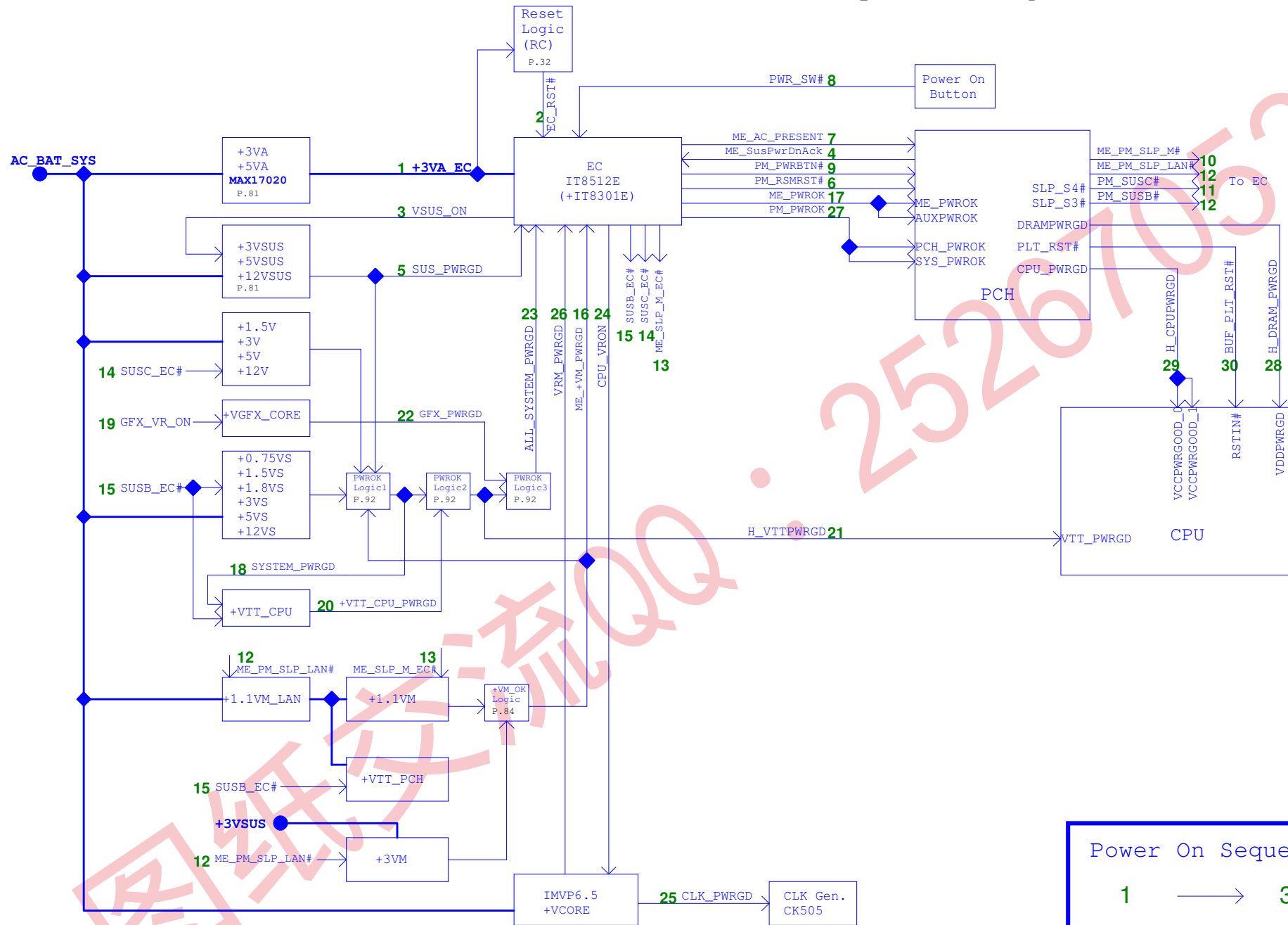




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PEGATRON			Title :	****
BU2/RD1			Engineer:	Gary Tsai
Size	Project Name		Rev	
Custom	G60J		1.1	
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# Power On Sequence Diagram Rev. 0.2



Power On Sequence

1 → 30

# Power-On Sequence Timing Diagram Rev. 0.2

